Agile Bandpass Sampling RF Receivers for low power Applications

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A Luma,
A ma famille
et à ceux qui me sont chers.

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Contents

Chapter 1 : Introduction

1 The Emerging Needs for Agile and Low Power RF Transceivers

1.1 The WPAN, WBAN and WS&AN - A Multitude of Low Power Applications on the ISM Band

The *Wireless Personal Area Network* (WPAN) is limited to some tens of meters range (<100m) and low- to medium- data rate (< 3 Mbps). Furthermore, the WPAN has evolved and led to the consideration of other networks such the *Wireless Body Area Network* (WBAN) and *Wireless Sensor & Actuator Network* (WS&AN). WPAN applications have been standardized by the 15th working group of IEEE802 and is split in 7 task groups. The low data rate WPAN defines the 4th task group leading to the IEEE802.15.4 specifications, whereas Bluetooth had been considered by the first task group, therefore IEEE802.15.1. Primarily, it was created to link small devices and peripherals with a computer, not specifically for data transfer, although in some applications this data is processed and further sent to a wider network. Following the publication of 802.15.1-2005, the IEEE Study Group 1b voted to discontinue their relationship with the Bluetooth SIG. Later versions of Bluetooth are not IEEE standards. Therefore the Bluetooth Low Energy that we apply in our study is not part of the IEEE802.15 working group.

The Bluetooth standard was created in 1994 by Ericsson. It was defined for a data rate around 1 Mbps and 30m communication distance range. Lately, the Bluetooth 2.0 EDR extended the data rate up to 3 Mbps. The Bluetooth standard is particularly adapted to file transfer applications and connections between a PC and peripheral appliances, known as *Piconet*, where up to 8 devices can be connected in this network. The first device is the master and all the other devices are slaves communicating with the master. As mentioned before, Bluetooth got apart from IEEE in 2005 and developed its own solutions in the WPAN area. Lately, it was perceived that the Bluetooth devices and specifications were not optimized in terms of power consumption, mostly for lower distances applications (up to 10m).

The concept of *Wireless Body Area Network* (WBAN) was created mainly for medical and sport applications, such as heart beat monitoring and other body condition status. In this application the data rate is not the main issue but the service quality is very demanding. The most recent version, Bluetooth 4.0 integrates a low power section specification called *Bluetooth Low Energy* (BT-LE) which objective is mainly to increase battery life for communication devices in the WBAN context. This work is focused on the low power configuration of Bluetooth. On the IEEE802.15 side, the concept of WBAN was also explored. Created in 2007, the task group IEEE802.15.6 is developing a communication standard optimized for low power devices, operating around the human body (but not limited to humans) covering a variety of applications, such as medical, Consumer Electronics, personal entertainment to name a few. In this case, there is a direct competition in terms of applications and band in use (the advantage of IEEE802.15.6 compared to BT-LE is to cover various bands other than the 2.4 GHz *Industrial, Scientific and Medical* (ISM) band).

As previously mentioned, the IEEE802.15.4 was created by the 4th IEEE802.15 task group. It was particularly interested in low data rate and high latency times. These characteristics are also well adapted to low cost, ultra low power and low data rate applications. It started to be widely used in industrial processes, now moving from *Wireless Sensor Network* (WSN)to *Wireless Sensor & Actuator Network* (WS&AN), where the network configuration is automatically set with the addition / suppression of nodes on the network. The IEEE802.15.4 is historically also applied for medical applications on the WBAN context [1]. The standard occupies three different bands: 868MHz (Europe), 915 MHz (USA) and 2.4 GHz worldwide.

The motivation on multistandard applications comes from the variety of *Physical Layer Device* (PHY) and *Media Access Control* (MAC) layers specifications in the 2.4 GHz ISM band, and even wider variety of specifications from the network layer protocols (Layer 3) to upper layers which can run over IEEE802.15.4-based networks, including ZigBee. Observing this promising field of applications, and considering that the 2.4 GHz ISM band is in most cases addressed by these standards, we propose to develop innovative receiver architecture capable of addressing this variety of standards in the WPAN, WBAN and WS&AN context. The most remarkable standard technologies for short range, IEEE802.15.4 and Bluetooth Low Energy, are the starting references for this work.

1.2 Technological Trends towards Discrete Time Signal Processing: On the Interest of Bandpass Sampling

RF transceivers that require a lot of analog components do not fully benefit from technological scaling. As a consequence, analog blocks and base band blocks such as *Digital Base Band Processor* (DBB) and the *Application Processor* (APP) do not progress similarly, the latter being best-adapted to deep-submicron technologies scaling. In such technologies, the strongest drawback limiting analog functions performances are the low voltage supply and high threshold voltages. In other words, there is considerable reduction on the voltage headroom to implement analog functions. On the other hand, the improvements on the switching characteristics of MOS transistors offer excellent time accuracy, and lithography offers precise control on the capacitance ratios [2]. Considering these trends, Mitola first envisaged the concept of *Software Defined Radio* (SDR) [3]. All the RF and base band stages are digital, through the application of an *Analog to Digital Converter* (ADC) directly connect to the antenna. It is evident that the ADC required performances should fulfill extraordinary specifications, and in this case becomes incompatible with the mandatory energy-efficient context. Although digital communication standards occupy frequency bands from 800 MHz to 6 GHz, the bandwidth of a single channel, goes to a maximum of 20MHz, apart from *Ultra Wide Band* (UWB) standards. Therefore, demodulation and base band processing can be reduced to this frequency in order to have multistandard digital circuitry. Signal processing operations prior to the ADC can be actually reduced to amplification, filtering and downconversion.

The idea to merge SDR concepts with power consumption constraint considerations and consists in using Discrete-Time receivers. One major argument is the possibility to exploit the natural technological scaling trend, while avoiding the weaknesses, such as reduction of voltage headroom or increasing technology variability ([2]-[4]). Theses trends are summarized and

detailed in [5]. Analog discrete-time circuits, such switched-capacitor networks, are adapted to implement the amplification, down-conversion and filtering operations mentioned above.

A particular interesting process that can be exploited on the context of Discrete Time receivers is the *Bandpass Sampling* (BPS). The BPS is one kind of Discrete Time receiver which permits conversion from *Continuous Time* (CT) domain to *Discrete Time* (DT) domain while also operating the down-conversion. The application of this principle is also motivated by the fact that the useful information occupies a bandwidth which is considerably lower than the carrier frequency. The front-end samples only the useful information, making possible to reduce both frequency synthesis and circuit cutoff frequencies. In order to apply the BPS and DT signal processing concepts into low power applications, it is even more interesting to further reduce the sampling frequency by applying high under-sampling ratio combined to anti-aliasing filters prior to the sampler Once the signal is in DT domain, process such as DT filtering, based on the principle of capacitance charge sharing, and decimation, can be applied to reduce the sampling frequency and to reject unwanted signals / interferers. Finally, these techniques enable the reduction of the ADC constraints in terms of clock frequency and resolution.

The new challenges when designing BPS receivers come from the aliasing of the spectrum while under-sampling and processing decimation. An optimized frequency plan has to be designed as well as some filtering techniques to overcome interferer's aliasing into the band of interest. Another considered aspect is to simplify the filtering networks by merging CT and DT filter techniques. We present in this work new methodologies and simulation tools able to address these various system level challenges in order to propose a new BPS architecture oriented to low power consumption and multi-standard purposes. The idea of designing a DT reconfigurable and low power receiver merges the technology trends towards the deep-submicron technologies and the evolution on the WPAN 2.4GHz ISM applications and standards.

2 Presentation of the Thesis Work

The objective of this thesis work is to propose and specify new receiver architectures able to address characteristics of both agile multi-standard and ultra low power receivers, exploring the BPS technique. In CHAPTER 2, the BPS theory is presented. We highlight the new challenges in terms of the system level design that the BPS process unveils. An overview of the various RF DT receiver architectures is presented. The idea is to set some original ways for down-conversion and filtering based on DT signal processing by merging different solutions and bringing the best of each, exploiting current available literature. On the following, the critical blocks state of the art in the receiving path is presented. The performances of the state of the art set the reference for low power system level design. CHAPTER 3 presents a system level simulation tool developed in MATLAB. Wide-band modeling is implemented to take into consideration the specificity of BPS receivers. A system level specification method which rapidly converges to the standard requirements is also presented. Using the proposed method and associated tool, a quantitative comparison has been carried out for different BPS architectures and is presented in CHAPTER 4. The system level design and block specifications over the

various architectures permit to have more insight on the DT architectures trade-offs. A particular attention is brought on the filtering optimization of the receiver chain between the continuous time elements (BAW, Lamb filters) and discrete time elements (switched capacitor active or passive networks). The carried out study ends by a proposition of a new RF BPS receiver architectures based on a high intermediate frequency and a complex DT filtering, regarded as the best trade-off between power consumption and agility. The derived block specifications are compared to the state of the art of the CHAPTER 2 in order to strengthen the work towards a low power goal.

The complex DT filtering function presenting Infinite Impulse Response (IIR) is a key component of the proposed architecture. This filter has a reduced order for a high selectivity and rejection performance while avoiding drawbacks coming from zero IF architectures, such 1/f noise, DC-offset, I/Q mismatches and second order non linearity. CHAPTER 5 presents the theory of DT filtering and its implementation on silicon. The objective of CHAPTER 5 is to validate the DT filter and to evaluate the impact of circuit implementation imperfections on the required frequency response. To achieve this goal, two approaches were adopted, analytical development on the imperfections and behavioral modeling simulation. The analytical approach is defined in terms signal and noise, in order to dimension capacitance sizes. From there, the behavioral modeling is applied further evaluate the circuit imperfections such as parasitic capacitances and non-linear parameters.

Chapter 2 : The Bandpass Sampling Process & the State of the Art

1 Introduction

The DT receiver is being presented in the literature as an interesting method to merge the technological down scaling trend to further improve integration and the need for agile multi-standard transceivers. The objective of this thesis work is at the same time to optimize the concept of DT receiver on the multi-standard aspect and to improve the power consumption for low power RF communications such as WPAN, WBAN and WS&AN. The technique of BPS is being presented here as a solution to alleviate the frequency synthesis constraints thanks to the implementation of the down-conversion process and a CT to DT conversion.

Considering the DT-based architectures, BPS operation and DT signal processing like filtering and decimation are merged into the whole chain through down-conversion and filtering. This chapter focuses on the theory of BPS. New challenges in terms of system level design come with the application of BPS. Two different techniques are possible during the sampling process: the voltage sampling and the charge sampling. This chapter highlights the difference between both techniques.

Concerning the architecture itself, the frequency plan can be defined in different ways with regards to BPS and DT filtering techniques, depending on preferred options e.g.; oriented towards multi-standard or low power applications for instance. In this chapter, the *State of the Art* (SOA) of the DT receivers is presented. We define a classification method based on the down-conversion process, the frequency plan and filtering techniques. Three orthogonal families of DT receivers can be mentioned in the SOA. They are compared in terms of agility and power consumption characteristics. The distinct BPS configurations defined in this chapter are further applied in the ISM band and the *Ultra Low Power* (ULP) standards, in order to lead a quantitative comparison in Chapter 4.

In this chapter, since the system level design of this work is low power oriented, we study the SOA on blocks whose power consumption is critical in RF transceivers. This includes the *Low Noise Amplifier* (LNA), Mixer, *Sample-and-Hold* (S/H) blocks, but also the frequency synthesis ones such as *Phase-Locked Loop* (PLL) and *Delay-Locked Loop* (DLL). The scope of this SOA concerns the 2.4GHz ISM band. Furthermore, on the system level design, the derived specifications provided in Chapter 4 will be compared to the retrieved SOA performances in order to demonstrate the feasibility of the proposed DT architectures in a low power context.

2 The Bandpass Sampling

2.1 Theoretical analysis

The conversion from the analog to the digital domain is composed by two distinct operations: first from continuous time to discrete time domain and then from continuous amplitude to discrete amplitude domain. Sampling a signal means observing a given value from a continuous time waveform at a given time instant. During the uniform sampling process the values of the

waveform are observed at the instants nT_S, where T_S is called the sampling period. The sampling process is modeled by two distinguished operations: the multiplication of the input signal $v_{in}(t)$ (Figure 2-1) by an infinite sequence of Dirac pulses, and a discretization in time and frequency domain [6, 7]:

$$v_{in\_S}(t) = v_{in}(t)\sum_{n=-\infty}^{\infty}\delta(t-nT_S) = \sum_{n=-\infty}^{\infty}v_{in}(nT_S) \tag{2-1}$$

$$V_{in\_S}(f) = V_{in}(f) * \frac{1}{T_S}\sum_{n=-\infty}^{\infty}\delta(f-nf_S) = \frac{1}{T_S}\sum_{n=-\infty}^{\infty}V_{in}(f-nf_S) \tag{2-2}$$

The convolution by a sequence of Dirac pulses in the frequency domain means that the sampled signal is periodic in frequency at $fs=1/T_S$ (2-2) (Figure 2-5). The signal $v_{in\_s}(t)$ (Figure 2-1) is still defined in CT-domain. The second operation is the discretization of $v_{in\_s}(t)$ to $v_{in}[n]$. While applying the DT Fourier Transform, we observe the discrete spectrum with a normalized frequency range $r=f/fs$. Lately, we show that the DT signal processing is not exclusive of the digital domain (discrete amplitude), but also possible on the analog domain (continuous amplitude). The sampled spectrum in the normalized frequency "r" domain is obtaining by substituting $f=r\cdot f_S$:

$$V_{in\_S}(r\cdot f_S) = V_{in}(r\cdot f_S) * \frac{1}{T_S}\sum_{n=-\infty}^{\infty}\delta(fs(r-n)) \tag{2-3}$$

From the scaling property of the Dirac delta function [8] which defines:

$$\delta(fs(r-n)) = \frac{\delta(r-n)}{|fs|} \tag{2-4}$$

We infer that the scaling coefficient 1/Ts disappears on the DT spectrum. Defining $V_{in\_S}(r)=V_{in\_S}(r\cdot fs)$, we have:

$$V_{in\_S}(r) = V_{in}(r) * \sum_{n=-\infty}^{\infty}\delta(r-n) = \sum_{n=-\infty}^{\infty}V_{in}(r-n) \tag{2-5}$$

The important difference is that the scaling factor $1/T_S$ only exists in CT domain, and disappears after the CT-to-DT conversion [6]. The Bandpass Sampling, also known as sub-sampling, considers a sampling frequency which does not respect the strict Nyquist-Shannon Criterion [9, 10] $fs>2\cdot f_H$, where f_H is the highest frequency of the signal to be sampled. The BPS theory is a generalized interpretation of the Nyquist-Shannon Theorem [11]. A bandpass signal $v_{in\_RF}(t)$ is a signal where the PSD $V_{in\_RF}(f)$ is centered at a given center frequency f_0 (Figure 2-4) with a bandwidth BW_{CH} much lower than this f_0 (Figure 2-4). The signal is bandpass sampled $v_{in\_RF\_s}(t)$, respecting the Nyquist-Shannon criterion $fs>2\cdot BW_{CH}$. The signal PSD is again periodic at fs (Figure 2-6) with an image of the signal falling into the lower band, the base band or an intermediate frequency.

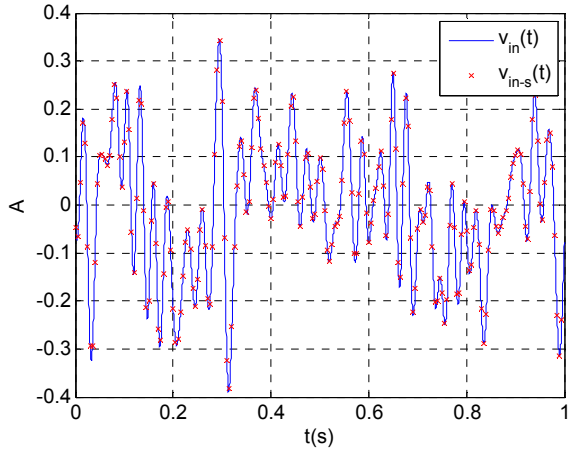


Figure 2-1 : The base band signal over sampled: $v_{in}(t)$ and $v_{in\_s}(t)$ (fs=200Hz)

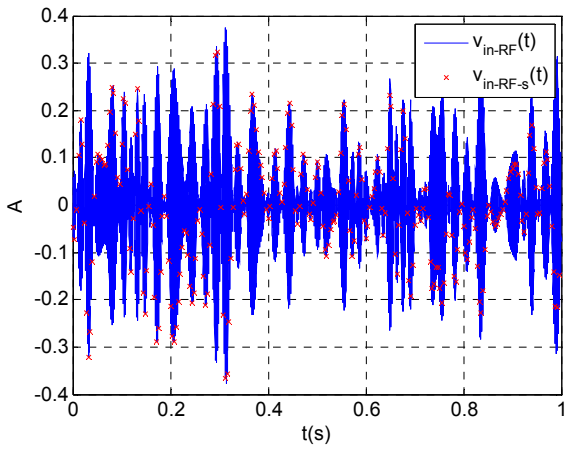


Figure 2-2 : The bandpass signal under-sampled: $v_{in\_RF}(t)$ f_0=500Hz (fs=250Hz)

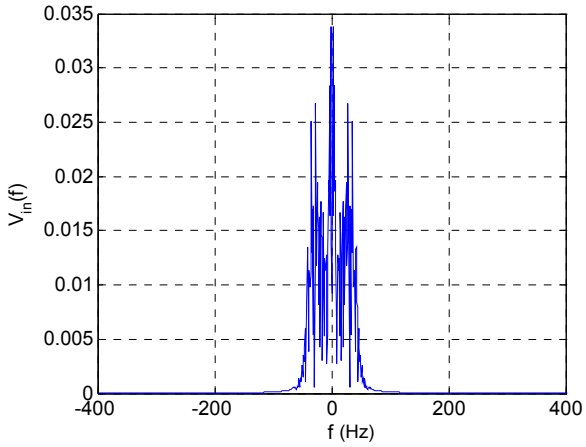


Figure 2-3 : $V_{in}(f)$

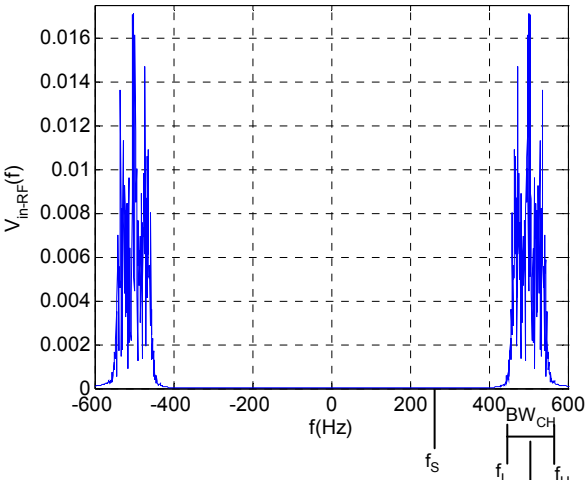


Figure 2-4 : $V_{in\_RF}(f)$, f_0=500Hz

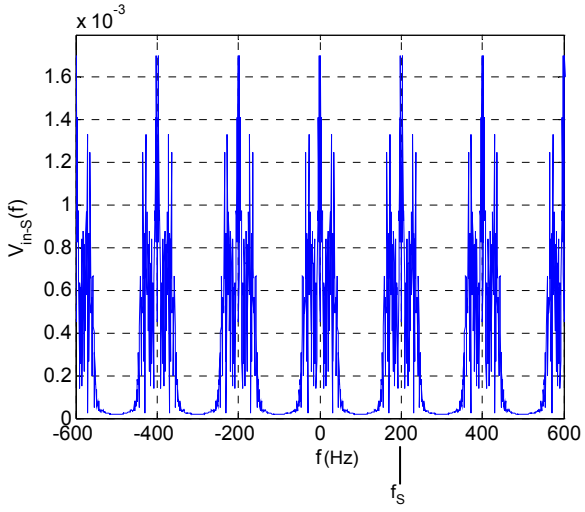


Figure 2-5 : $V_{in\_s}(f)$ f_0=0, fs=200Hz

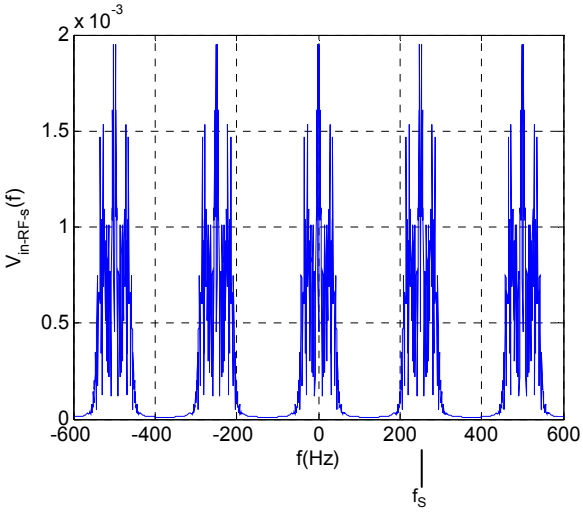


Figure 2-6 : $V_{in\_RF\_s}(f)$, f_0=500Hz, fs=250Hz

Figure 2-1 illustrates the base input signal along with the sampled values according to the Shannon-Nyquist criterion. In Figure 2-2, the same signal is converted to f_0=500Hz and Bandpass Sampled. The sampled signal PSD $V_{in\_s}(f)$ is given in Figure 2-5 : it is continuous and periodic at fs. In Figure 2-2, the signal input $v_{in\_RF}(t)$ is modulated by a carrier at f_0=500Hz (Figure 2-4). The signal is Bandpass Sampled compared to the carrier at fs=250Hz, leading to the

same sampled signal from the Nyquist sampling. The sampled spectrum is periodic at fs=250Hz (Figure 2-6). In both Figure 2-5 and Figure 2-6 the spectrum around the base band is the same (scaled by 1/Ts). From expression (2-5), the scaling faction 1/Ts is suppressed.

Figure 2-7 illustrates the bandpass sampled signal down-converted to the base band. The spectrum is periodic at fs, and an image of the signal at RF is convolved to the base band, and the input signal is band limited by f_L and f_H (Figure 2-7 (a)). From Figure 2-7 (b), the lowest distance between n·fs/2 (n being even) and the center frequency of the signal sets the Intermediate Frequency (IF) of the down-conversion Figure 2-7 (c). In other words, the convolution between the Dirac pulse placed at n·fs/2 and the RF signal sets the base band signal.

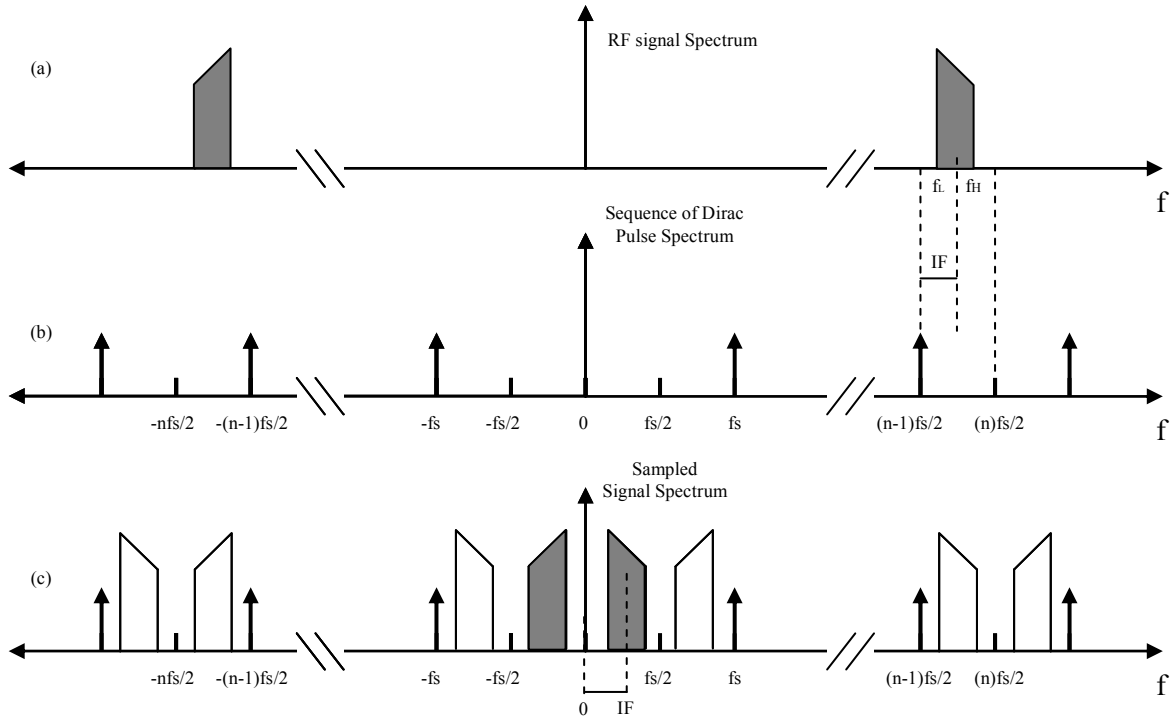


Figure 2-7 : Frequency representation of the BPS process ; (a) the RF signal, (b) the Dirac pulses sequence, (c) the bandpass sampled signal

Observing the frequency plan presented in Figure 2-7, the following relations have to be respected in order to avoid spectrum aliasing. The value "n" is defined as the under-sampling ratio ([11]):

$$n = 2 \cdot \frac{f_H}{f_s} \tag{2-6}$$

$$\frac{(n-1)\cdot f_s}{2} < f_L \tag{2-7}$$

$$\frac{(n)\cdot f_s}{2} > f_H \tag{2-8}$$

$$\frac{2f_H}{n} \le f_S \le \frac{2f_L}{n-1} \tag{2-9}$$

The maximum allowed bandwidth is therefore derived from (2-9):

$$BW_{\max} = \min\{2f_0 - (n-1)fs \quad , \quad n\cdot fs - 2f_0\} \tag{2-10}$$

The first advantage on the BPS is the down-conversion in the frequency domain and the time discretization of the signal on the same process. The second one is that low sampling frequencies can be applied in order to relax frequency synthesis. The discrete-time signal processing can still be applied in analog domain (discrete-time with continuous amplitude) in order to implement filtering process and decimation functions. These filters are referred in this thesis work as Discrete-Time filters and filters applied after the ADC are defined as Digital filters.

The drawback of the BPS process is the spectral folding of undesired signal into the band of interest (Figure 2-8 (a)). For instance, we have to consider the thermal noise, limited in a band BW_{noise} which represents the cut-off frequency of the sampling system. In a sampling system, the periodicity of the spectrum implies that the wideband noise folds into each of the fs/2 bands [11]. Before sampling, consider the in-band continuous time noise PSD defined as N_{C_PSD} (Figure 2-8) and the out-of-band noise PSD defined as N_{C_PSD}/Δ_{noise}, where Δ_{noise} is capacity of filtering the input noise prior to sampling. The sampled noise PSD is defined as PSD_{S_PSD} (Figure 2-8 (b)). The increase of noise PSD between before and after sampling process is defined as the aliasing factor, $\gamma=N_{out\_PSD}/N_{in\_PSD}$ (Figure 2-8 (b)).

The signal-to-noise ratio of the sampled signal is degraded by at least the aliased noise from DC to $BW_{noise.}$ Thereafter, to reduce the impact of γ, an anti-aliasing filter is applied which rejects the out-of-band noise by Δ_{noise}. The resulting aliasing factor is defined as :

$$\gamma = 1 + \frac{2 \cdot BW_{noise} / \Delta_{noise}}{fs} = SNR_{deg} \qquad (2\text{-}11)$$

In BPS, the N^{th} harmonic of the Dirac pulses defines the down-conversion (Figure 2-8 (a)). The distance between the N^{th} harmonic and the signal of interest sets the Intermediate Frequency IF after sampling. In a wideband spectrum context, there can be multiple interferers folding into the band, when their frequency distance to another multiple of the sampling Dirac is also IF (Figure 2-8 (b)) : they are aliasing interferers or image interferers.

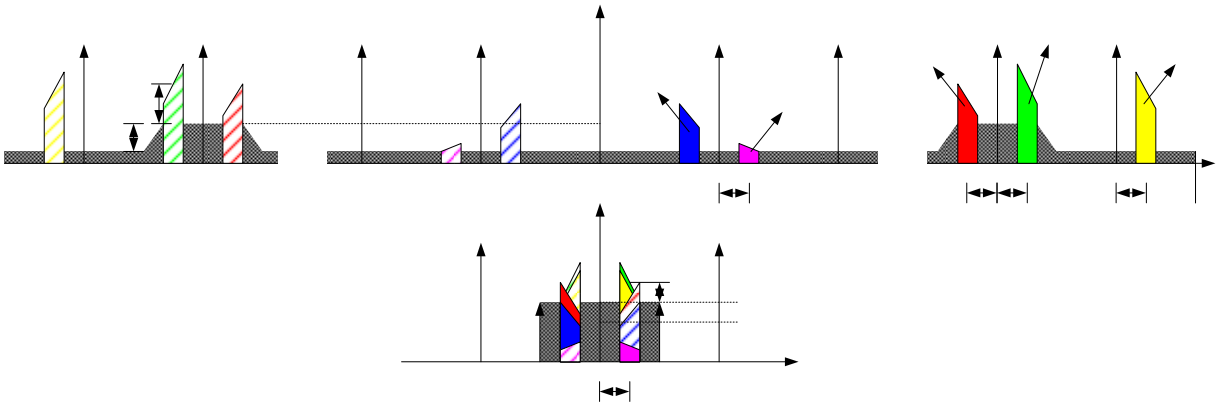


Figure 2-8 : The BPS: the spectrum before (a) and after (b) sampling

The spectrum aliasing represents the most important constraint to consider when designing BPS architectures. The accurate knowledge of the aliasing bands enables the definition of filtering techniques and frequency plan, considering the given application and specifically its frequency band in use.

2.2 The voltage and charge sampling

There are two methods to implement the sampling operation at the circuit level: the *Voltage Sampling* and the *Charge Sampling*. Voltage sampling is a conventional method which is implemented by *Sample-and-Hold* (S/H) circuit. It tracks an analog signal and stores its value as a voltage in a sampling capacitance, and keeps this voltage for some length of time. The *Charge-and-Hold* (C/H) circuit integrates the signal current within a given window. The input is transferred from voltage to charge domain before it is sampled. In the next sections, we derive the sampling transfer function in order to show the basic differences between these two techniques ([12]). The output noise divided to *Gain Bandwidth* (G · BW) is derived to compare the relations between noise and power consumption for both techniques.

2.2.1 Voltage Sampling

Ideally, a voltage sampling can be modeled as the input voltage signal sampled by ideal sampler (2-1). Actual implementations use the S/H block presented in Figure 2-9. The samples are considered at all nTs times. The sample is Hold between nTs and nTs+τTs, (τ is the duty cycle $0<\tau<1$). During the Hold period, the signal can be quantized by an ADC or DT analog signal processing can be implemented (i.e. DT filters). The next sample is tracked from nTs+τTs to (n+1)Ts. At (n+1)Ts , the next sample is considered. If, in the tracking phase, the exact value of $v_{in}(t)$ is hold, the sampled DT signal is the same than as defined in (2-1). On the other hand, during the tracking phase, the switch ON resistance R_{ON} and the sampling capacitance Cs represent a low-pass filter between $v_{out}(t)$ and $v_{in}(t)$ (Figure 2-9), defined in the frequency domain as H(f):

$$H(f)=\frac{1}{1+j2\pi\cdot f\cdot R_{ON}C_S} \tag{2-12}$$

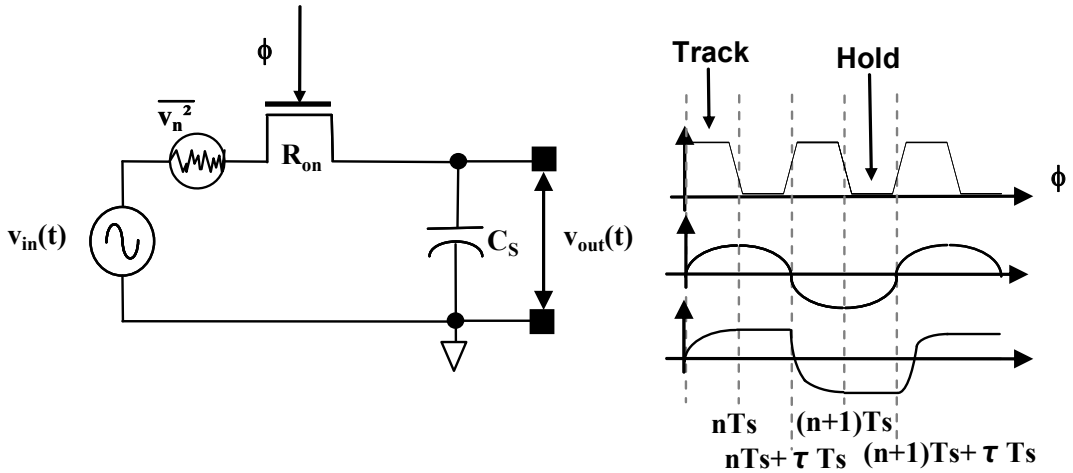


Figure 2-9 : The Sample-and-Hold circuit and the clock scheme

The sampled signal is therefore defined by:

$$V_{out\_S}(r)=\sum_{n=-\infty}^{\infty}V_{out}(r-n)=\sum_{n=-\infty}^{\infty}V_{in}(r-n)\cdot H(r-n) \tag{2-13}$$

In conclusion, the discrete time sequence is the application of the sampling process of a low-pass filtered Continuous Time signal.

2.2.1.1 Input Referred Noise and the Gain Bandwidth Product.

The noise generated by the S/H circuit is defined by the switch resistance R_{ON} and the circuit cut-off frequency. The total noise is the generated PSD noise integrated along the frequency:

$$v_n^2\left(V^2\right)=\int_0^{\infty}4\cdot K\cdot T\cdot R_{ON}\cdot\left|H(f)\right|^2 df=4\cdot K\cdot T\cdot R_{ON}\cdot\int_0^{\infty}\frac{1}{1+\left(2\pi\cdot f\cdot R_{ON}C_S\right)^2}df$$

$$v_n^2\left(V^2\right)=\frac{KT}{C_S} \tag{2-14}$$

$$PSD_{S/H}\left(V^2/Hz\right)=\frac{K\cdot T}{C_S}\cdot\frac{2}{fs} \tag{2-15}$$

where k is the Boltzmann Constant, T is the temperature in Kelvin and fs=1/Ts. The input referred noise depends on the process gain on the sampling level. Consider a buffer presenting a transconductance "gm" and a unit load resistance; we observe the *Gain Bandwidth* (G·BW) (in hertz) product:

$$GBW=\frac{gm}{2\pi C_S} \tag{2-16}$$

The output noise-to-gain bandwidth ratio is defined as follows:

$$\frac{PSD}{G\cdot BW}=\frac{4\pi^2 C_S^{\,2}}{gm^2}\cdot\frac{K\cdot T}{C_S}\cdot\frac{2}{fs} \tag{2-17}$$

What is observed is that power consumption (in this case represented by gm) will depend on the required input referred noise figure and gain. In this section, it is shown that the choice for the sampling capacitance and for the transconductance gain infers the sampling system bandwidth, gain and noise. Small capacitances lead to high noise at constant power consumption. A third aspect is the sampling frequency which folds the KT/C noise in the fs/2 band.

2.2.2 Charge Sampling

In charge sampling, the voltage is transferred into a current source, and it is integrated in C_S between nTs-Δt and nTs (Figure 2-10). The integrated value is therefore held and reset; the charging integration restarting at (n+1)Ts-Δt.

The sampled voltage is defined as [13]:

$$v_{out}(nTs)=\frac{1}{Cs}\int_{nTs-\Delta t}^{nTs}gm\cdot v_{in}(t)dt=\frac{1}{Cs}\int_{-\infty}^{\infty}gm\cdot v_{in}(t)\cdot\left[u\left(t-\left(nTs-\Delta t\right)\right)-u\left(t-nTs\right)dt\right] \tag{2-18}$$

where u(t) is the unit step function. Now, let consider $f_0(t)$ defined as:

$$f_0(t)=u(-t+\Delta t)-u(-t) \tag{2-19}$$

The equation (2-18) becomes:

$$v_{out}(nTs)=\frac{1}{Cs}\int_{-\infty}^{\infty}gm\cdot v_{in}(t)\cdot f_0(nTs-t)dt=\frac{gm}{Cs}\cdot\left[v_{in}(t)*f_0(t)\right]\cdot\delta(t-nTs) \tag{2-20}$$

$$v_{out}(t)=\frac{gm}{Cs}\cdot\left[v_{in}(t)*f_0(t)\right]\xleftrightarrow{\Im}V_{out}(f)=\frac{gm}{Cs}\cdot V_{in}(f)\cdot F_0(f) \tag{2-21}$$

Similar to H(f) defined in (2-12), $F_0(f)$ represents the frequency response for the filtering function prior to sampling [13]:

$$F_0(f) = \Delta t \cdot \mathrm{sinc}(\pi f \Delta t) \tag{2-22}$$

Similarly to (2-5), the DT spectrum of the charge sampled signal is given by:

$$V_{out\_S}(r) = \sum_{n=-\infty}^{\infty} V_{in}(r-n) \cdot \frac{gm}{C_S} \cdot F_0(r-n) = \sum_{n=-\infty}^{\infty} V_{in}(r-n) \cdot \frac{gm \cdot \Delta t}{C_S} \cdot \mathrm{sinc}(\pi(r-n)\Delta t) \tag{2-23}$$

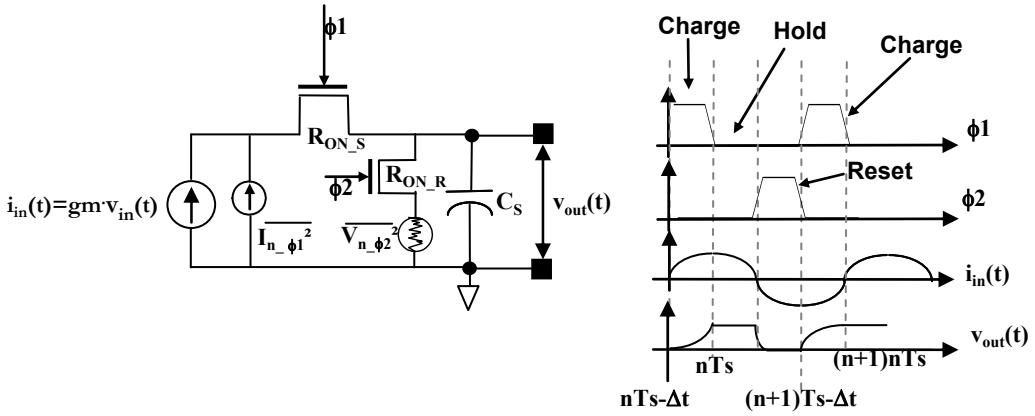


Figure 2-10 : The Charge-and-Hold circuit and the clock scheme

The sinc function is an intrinsic filtering function on the charge integration, which can be considered as an anti-aliasing function. As the voltage sampling is limited by the gm and the Cs from the intrinsic low-pass function on the S/H circuit; the charge sampling is limited by Cs and gm integration process, which also represents a low-pass behavior. The cut-off frequency depends on the integration period Δt (and therefore on the clock), contrarily to the RC time constant for the voltage sampling. The filtering stage (H(f) $F_0(f)$) is applied prior to sampling, therefore the filtering transfer function stages are not periodic. On the sampling process the filtered signal becomes periodic.

2.2.2.1 Input Referred Noise and the Gain Bandwidth Product.

During the charging phase, the R_{ON} resistance from the sampling switch R_{ON_S} is seen as a current noise source, which is integrated in the defined window $F_0(f)$. The noise from the sampling switch is defined as follows:

$$v_{n\_\phi 1}^2(V^2) = \int_0^{\infty} \frac{4 \cdot K \cdot T}{R_{ON\_S}} \cdot |F_0(f)|^2 df = \frac{K \cdot T}{C_S} \cdot \frac{2\Delta t}{R_{ON\_S} C_S} \tag{2-24}$$

The reset switch of Figure 2-10 also contributes to the noise level. During the charging phase, the noise from the reset switch is discharged (the time constant depending on the sampling switch R_{ON_S}), and at the beginning of the hold phase, it is added to the sampling switch noise:

$$v_{n\_\phi 2}^2(V^2) = \int_0^{\infty} 4 \cdot K \cdot T \cdot R_{ON\_R} \cdot \frac{1}{1+(2\pi R_{ON\_R} C_S)^2} \left(e^{-\Delta t/(R_{ON\_S} C_S)}\right)^2 df = \frac{K \cdot T}{C_S} \left(e^{-2\Delta t/(R_{ON\_S} C_S)}\right) \tag{2-25}$$

Therefore, the total output noise PSD is given by:

$$PSD_{C/H}\left(V^2/Hz\right)=\frac{K\cdot T}{C_S}\cdot\frac{2}{fs}\cdot\left(\frac{2\Delta t}{R_{ON\_S}C_S}+\left(e^{-2\Delta t/\left(R_{ON\_S}C_S\right)}\right)\right) \tag{2-26}$$

The filtering function of the charge sampling is defined by (2-21). The cut-off frequency is independent on the $R_{ON\_S}C_S$ time constant, but on the integration interval Δt (when $\text{sinc}(\pi f\Delta t)=0.71$, i.e. $\pi f\Delta t=\pi\cdot 0.44$). The noise becomes scaled by the $\Delta t/R_{ON}C_S$ ratio:

$$PSD_{C/H}\left(V^2/Hz\right)=\begin{cases}\dfrac{KT}{C_S} & if\ 2\Delta t << R_{ON\_S}C_S\\ \dfrac{KT}{C_S}\left(\dfrac{2\Delta t}{R_{ON\_S}C_S}\right) & if\ 2\Delta t >> R_{ON\_S}C_S\end{cases} \tag{2-27}$$

In order to compare this with the voltage sampling, we develop the expression for the noise divided by G·BW on the charge sampling process. The gain at DC for the charge sampling is given thanks to (2-22), $G=gm\cdot\Delta t/C_S$. The -3dB cut-off frequency is defined when $\pi fc\Delta t=\pi\cdot 0.44$ ($\text{sinc}(\pi fc\Delta t)=0.71$), which leads to $fc=0.44/\Delta t$. GBW is defined as follows:

$$G\cdot BW=\frac{gm}{Cs}\cdot 0.44 \tag{2-28}$$

$$\frac{PSD}{G\cdot BW}=\frac{C_S^{\,2}}{gm^2}\cdot\frac{KT}{C_S}\cdot\frac{2}{fs}\cdot\left(\frac{2\Delta t}{R_{ON}C_S}+\left(e^{-2\Delta t/\left(R_{ON\_S}C_S\right)}\right)\right)\cdot\frac{1}{(0.44)^2} \tag{2-29}$$

Better gain bandwidth is achieved by charge sampling for the same gm, where the noise can be as low as KT/C_S for high R_{ON_S}.

2.2.3 Comparative study summary

The following table summarizes the different characteristics of both sampling techniques:

Parameters	Voltage sampling	Charge sampling
BW(Hz)	$1/(2\pi R_{ON}C_S)$	$0.44/\Delta t$
Noise	$\%\ 1/C_S$	$\%\ \Delta t/(R_{ON}C_S)$
Realization	Simple	V-I Converter Resetting Structure
Anti-aliasing	LP filter	Sinc filter

Table 2-1 : The low power and/or wideband LNA SOA

The voltage sampling is mostly dependent on the RC time constant, and for high frequencies, the switch resistance is a critical parameter to consider. At Nyquist sampling, the $\tau=2\pi RC$ time constant is defined to be at least $\tau=1/(5\cdot f_H)$, where f_H is the highest frequency to be sampled. The H(f) (2-12) transfer function presents a non-constant group delay τ_g, which leads to signal distortion. Figure 2-13 illustrates (right hand axis) the variation of the group delay in percent. At Nyquist sampling, if the time constant is one fifth of the highest sampling frequency to be sampled ($\tau=1/(5\cdot f_H)$) $f_H=0.2\cdot fc$, from Figure 2-11 we observe that it represents a variation on the group delay of $\Delta\tau_g=3.7\%$. On the other hand, in BPS process, the band occupied by the signal is very small compared to the center frequency $f_0>>BW_{CH}$. For a signal centered at the cut-off frequency of the system $f_0=1/\tau$, the variation of $\Delta\tau_g=3.7\%$ is observed when $f_0/BW_{CH}=12.67$. In conclusion, the constraint to define RC time constant in BPS is reduced if compared to Nyquist sampling. In this case H(f) at f_0 can be seen just as losses in the sampling

process. It is important to notice that the voltage sampling transfer function is independent on the sampling frequency and on the duty cycle.

On the charge sampling, the transfer function is defined by a sinus cardinal where the cut-off frequency is dependent on the sampling interval Δt (Figure 2-10). The charge sampling needs a linear V-I converter and a reset stage, which leads to somewhat more complex circuits. The sinus cardinal function has the advantage of presenting a transfer function with linear phase, where the cut-off frequency can be closer to f_H for Nyquist sampling process. For the BPS it becomes a drawback since the transfer function depends on the applied sampling frequency. Considering a duty cycle of Δt·fs=0.5, if the signal center frequency is f_0=fs, the signal is already attenuated by a factor greater than 3dB. For higher frequencies the sinus cardinal filter will suppress the signal of interest. In order to reduce the sampling frequency, Δt has to be kept constant, and in this case, the duty cycle is changed. In any of cases the charge sampling becomes a constraint on the clock generation.

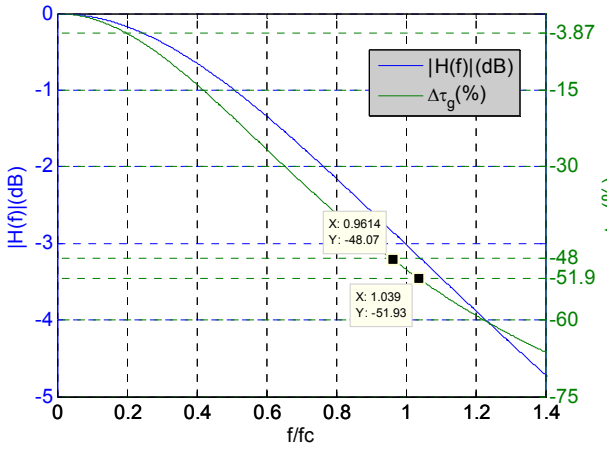


Figure 2-11 : The group delay relative variation in voltage sampling

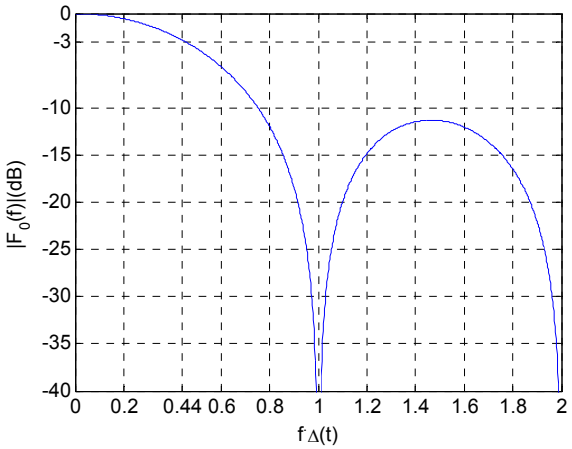


Figure 2-12 : The charge sampling sinc filter

In conclusion, if lower sampling frequencies and simple clock generation are aimed at, the voltage sampling has to be preferred. For high under-sampling ratios, implemented with either voltage or charge sampling, an anti-aliasing filter is mandatory to reduce the impact of the aliasing noise. The RC time constant drawback noticed in Nyquist operations is less constraining in BPS test cases when f_0>>BW_{CH}.

3 An Overview of RF Down-conversion and Filtering on Discrete-Time Architectures

3.1 Architectures Classification

In order to classify the various DT receiver architectures, we derive a generic mapping of the possible down-conversion and filtering techniques (Figure 2-13). The studied DT architectures in the literature are [2, 4, 6, 14-20]:

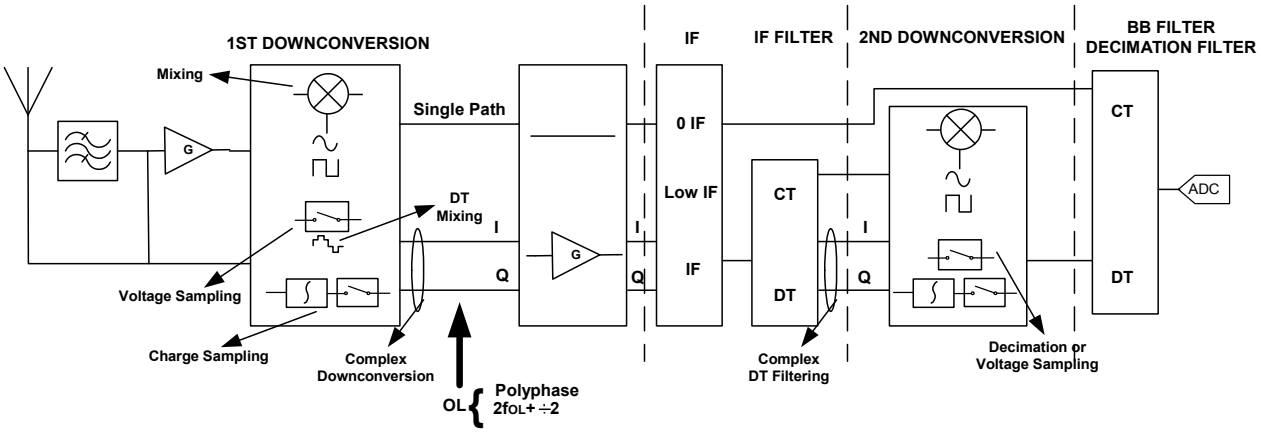


Figure 2-13 : – Synoptic of the down-conversion and filtering techniques.

In most cases, the RF filter is mandatory, since the linearity constraints on the LNA would be impossible to fit considering low power requirements. The idea in this work is to find the fair trade-off between reconfigurability and power consumption. *Software Defined Radio* architectures often use wideband LNAs without any RF filters [4, 6]. When non linear LNA's are employed, a bank of RF filters is needed to address multiple bands.

Frequency down-conversion can be implemented using classical mixer stages, where the Local Oscillator (LO) can present various waveforms. Different waveforms are implemented in order avoid harmonic intermodulation products. Charge sampling [2, 4, 15-17] and voltage sampling [6, 14, 18, 19] have also been implemented directly at RF frequencies. The first down-conversion can be implemented in single path or in quadrature. Three distinct groups appear in this classification:

- Nyquist-like sampling *Receiver* (RX) [2, 4, 6, 15, 16].
- RF/IF Bandpass Sampling with single path filters RX [14, 19, 20].
- RF/IF Bandpass Sampling with complex filtering RX [17, 18].

The first family of architectures presents a sampling frequency at least $fs=f_{RF}$. The minimum under-sampling ratio is n=2. We then refer this kind of process as Nyquist-like sampling RX. The second family exploits the properties of BPS in order to reduce the sampling frequency, while applying voltage sampling. Precise quadrature synthesis is needed for the complex sampling operation. The third family implements the concept of complex filtering in DT domain. The complex filter is used either to implement direct conversion with single clock generation or to implement image rejection at low-IF. On the following sections, the various receiving strategies from the SOA will be classified according to the generic scheme of Figure 2-13, and pros and cons are listed for each architecture family.

3.2 Nyquist-like sampling RX

The common point of all architectures in this family is the single down-conversion to zero- or low-IF. Quadrature frequency synthesis is therefore necessary to discriminate the receiving paths in the former case. The classification for such receivers is in Figure 2-14. Charge

and voltage sampling examples are present in this type of architecture. The related SOA for this architecture family is in [2, 4, 6, 15, 16].

The RF filter is suppressed in the case where several RF bands are desired; on the other hand more complicated DT filtering networks are implemented to achieve the required rejection and highly linear LNA are used. Although the inherent integration filter is capable to implement out-of-band anti-aliasing filtering, many out–of-band signals are still present from DC to f_{RF} which may saturate the amplifier stage and block the signal of interest.

Considering the inherent integration filtering of charge sampling [2, 4, 15, 16], the under-sampling ratio (2-6) is limited to 2, which leads to sampling frequencies as high as the RF center frequencies. The presented quadrature frequency synthesis blocks consist of a clock reference at $2 \cdot f_{RF}$ then followed by a divider-by-two. Thereby, considering the rising or the falling edges of this division process, the quadrature clocks are generated. This technique while improving I/Q mismatches compared to polyphase *Voltage Controlled Oscillator* (VCO) requires generating the base frequency at least at twice the RF frequency.

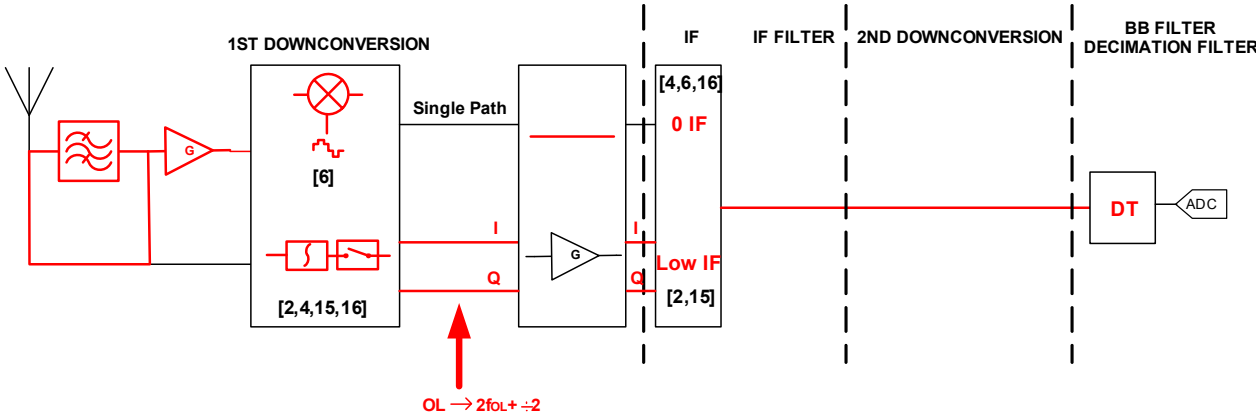


Figure 2-14 : – Down-conversion and filtering techniques for [2, 4, 6, 15, 16]

Over-sampling, and DT mixing is present in [6]. This technique allows applying *Harmonic Rejection* (HR) with a DT mixing process. In [6], the generated frequency is $fs=8 \cdot f_{RF}$, where 8 different phases define a sine/cosine pair. This technique improves anti-aliasing characteristics and harmonics intermodulation rejection. The selected gains are 1:√2: -√2:-1:-1:-√2:√2:1 for cosine wave and √2:1:1:√2:-√2:-1:-1:-√2 for sine wave. The DFT of this sequence leads to a signal where the 3rd and 5th harmonics are rejected.

For all receivers considered in this section, once the signal is down-converted, successive decimations down to the ADC sampling frequency are implemented. In order to avoid the noise / interferer aliasing in the band presented in Figure 2-8, consecutive DT filtering and decimation are implemented. There is a trade -off between the DT filter / decimation circuit complexity and the ADC performances. Higher ADC sampling frequency is present in [16], where more performing DT filtering techniques are presented in [4]. In this case, the filters orders or the number of decimation steps increase. Implementing DT filtering at high fs is sensitive to parasitic capacitances and represents a constraint on the clock tree generation (mismatch and clock buffers). Figure 2-15 and Figure 2-16 illustrate the power consumption distribution for [16] and [4], respectively. Notice that the clock and the synthesis power consumptions represents from 30% to 40% of the total receiver power.

At zero-IF, careful design is required to reduce 1/f noise, DC offset and second order non-linearity [4, 6, 16]. A low-IF frequency plan is preferred in [2, 15]. Both choices suffer from I/Q mismatch: at zero-IF, it leads to EVM degradation whereas at low-IF, it leads to finite image rejection. Apart from the drawbacks of zero-IF, low-IF presents a more constraining test bench regarding I/Q mismatch, considering that the image signal is an interferer which power is higher than the signal of interest one.

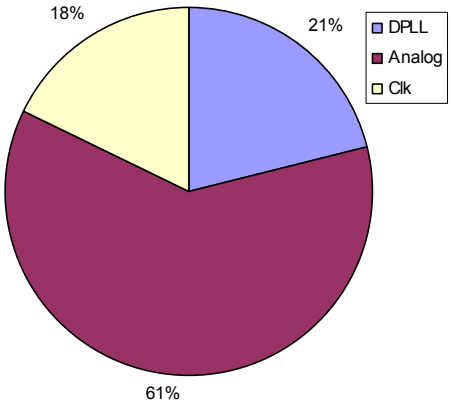


Figure 2-15 : – Power consumption Budget for [16]

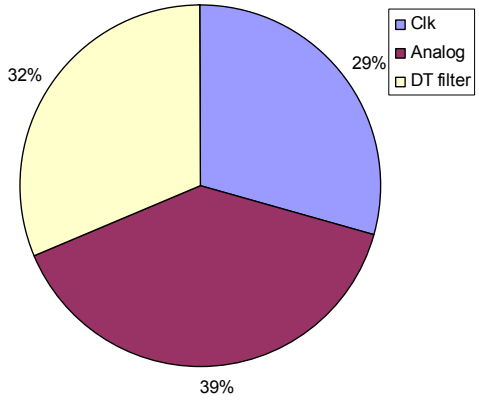


Figure 2-16 : – Power consumption Budget for [4]

The sampling frequency, which sets the down-conversion, changes for each channel to be addressed. Since constant decimation order is applied, the ADC works at a variable sampling rate. A fractional decimation is needed Between the ADC sampling frequency and the digital base band, where digital processors work at constant rate. The DT signal processing gives certain flexibility to the circuit. Consider the filtering function defined on the normalized frequency range. The filter notches are defined at multiples of the decimated frequency, meaning that they shift in absolute value with the sampling frequency. The ADC clock frequency can be reduced changing the decimation order. In conclusion, this family of architectures proposes a great agility to address various standards, considering that the reconfiguration relies on a wide frequency range synthesis and several filtering/decimation stages. A bank of RF front-end filters or highly linear LNAs are used, depending on the integration level / power consumption trade-off.

3.3 RF/IF Bandpass Sampling with Single Path Filters RX

In this case, low sampling frequencies are preferred, which implies that charge sampling is avoided. The voltage sampling S/H circuits are better adapted for that matter [14, 19, 20]. The classification for such receivers is illustrated in Figure 2-17:

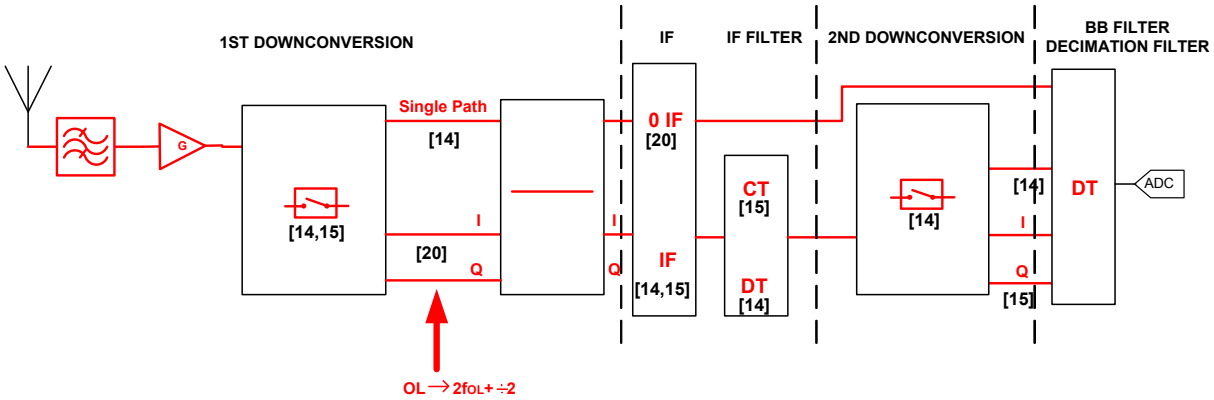


Figure 2-17 : – Down-conversion and filtering techniques for [14, 19, 20]

In order to reduce the sampling frequency, [20] the charge sampling becomes impractical since the inherent integration filtering rejects the signal of interest (as presented in section 2). Considering that the RF filter bandwidth correctly rejects out-of-band blockers, the sampling frequency can be reduced as low as BW_{RF}. For direct conversion, the quadrature clock at 2·fs is sensibly small compared with the previous architecture family. To correctly separate the I/Q signals, the under-sampling ratio is set as follows: (n/2) must be an odd number ([20]). Lately in Chapter 4, we will observe that this topology is even more sensitive to I/Q mismatch than if $fs=f_{RF}$. This is the case since the phase difference multiplies over the harmonics of fs. With a low sampling frequency and no intrinsic filtering, the voltage sampling with high "n" needs anti-aliasing filtering. For the thermal noise, smooth filtering is sufficient. For example the output noise of a tuned LNA presents low enough noise to support the aliasing factor. CT anti-aliasing at RF are implemented by *Surface Acoustic Wave* (SAW), *Bulk Acoustic Wave* (BAW), BAW *Lamb Wave Resonators* (LWR) and LC tuned LNA filters.

Single path sampling can be used to avoid problems from I/Q mismatch. In [19], the first BPS sampling operation is used for down-conversion. From the first sampling process the signal is down-converted from the RF frequencies to an IF. Consider the aliasing cases illustrated in Figure 2-8, the IF must be higher than the front-end filter BW to avoid image and out-of-band aliasing. The frequency plan is defined in such a way that a single sampling frequency (fs=761.8 MHz) is applied to down-convert three RF bands (GSM, UMTS and IEEE802.11g) to the same IF (114.6 MHz to 189.2 MHz) range. Since a single fs is applied, the IF band is as wide as the RF band. To address several channels, the second sampling frequency is variable inside the IF band. The decimation ratio between the first and the second sampling frequencies is mostly non integer. The simplest way to implement this decimation is to reconvert the signal from CT-domain to DT-domain, and then resampling. The CT-domain to DT-domain conversion is implemented by an interpolation filter at IF. The wide IF bandwidth is the main drawback of this architecture, since the filter needs a very large relative bandwidth ($BW_{IF}/IF\approx49\%$). The second sampling frequency is centered on the channel to demodulate. The complex IF sampling also suffers from I/Q mismatches, but at lower frequencies, this constraint is better overcome.

In [14], a higher under-sampling ratio of n=23 is considered, where an anti-aliasing filter is implemented at the LNA output. In this work, the same RF filter design is applied before and after the LNA. Both filters and the LNA are off-chip in this work. In [14], the sampling frequency is slightly higher than the RF BW. From the first sampling stage to the ADC, several DT filter and decimation stages are applied. The signal is down-converted to IF1=fs/3. The image signal at $f_{RF}+2fs/3$ is filtered prior to sampling by RF filtering techniques. From the first sampling frequency to the ADC clock frequency, several decimations by 2 are implemented. After the decimation process, the signal falls again at $fs_{dec}/3$, where fs_{dec} is the decimated sampling frequency. A possible interferer that is centered at fs/6 will also fall at $fs_{dec}/3$. The DT filter is implemented in such a way to have the pass band at fs/3 and a zero at fs/6. The chosen filter type is the Bi-quadratic filter ([14]) (IIR filter). The same DT filter can be used along with all decimation stages. Low-IF and low f_{ADC} can be achieved as long as the image rejection specification is met by the bi-quadratic filter.

This architecture family relies on reducing the sampling frequency while applying voltage BPS. Possible passive IF filtering for anti-aliasing can be implemented by BAW-Lamb filters and

SAW filters. The SOA on the filtering blocks is presented in section 4.4.2. The RF front-end filter is used as an interferers anti-aliasing filter, and tuned LNAs for noise anti-aliasing prior to sampling. Single path sampling to low-IF presented in [14] merges the sampling frequency reduction and relax 1/f noise, DC-offset and IIP2 constraints. The drawback is the DT filter implementation complexity.

3.4 RF/IF Bandpass Sampling with complex filtering RX

The complex demodulation presented in section 3.2 consists on having two sampling clocks which are shifted in phase by 90º, and, for the low-IF case study, on applying the complex sampling for image rejection. In section 3.3, single path sampling is applied with the image signal being rejected prior to sampling by a CT filter (at RF or IF). The complex sampling suffers from I/Q mismatch which will generate distortion at base band level in the case of zero-IF or limited image rejection in the case of low-IF. The image rejection implemented by CT filters is only achieved with selective filters or with relatively high IF.

In order to avoid I/Q mismatch issues from complex sampling process and to relax or suppress off-chip CT filters, the technique of complex DT filtering is implemented in [17, 18]. The main idea is to shift the frequency response of a low-pass DT filter into an intermediate frequency using the Hilbert Transform [21]. The theory of the DT filtering, and in particular the complex DT filtering, is presented in Chapter 5. The resulting filter contains complex coefficients and is non-symmetric from a frequency point of view, enabling to filter image frequency signals. The receiving strategy of [17, 18] is summarized in Figure 2-18:

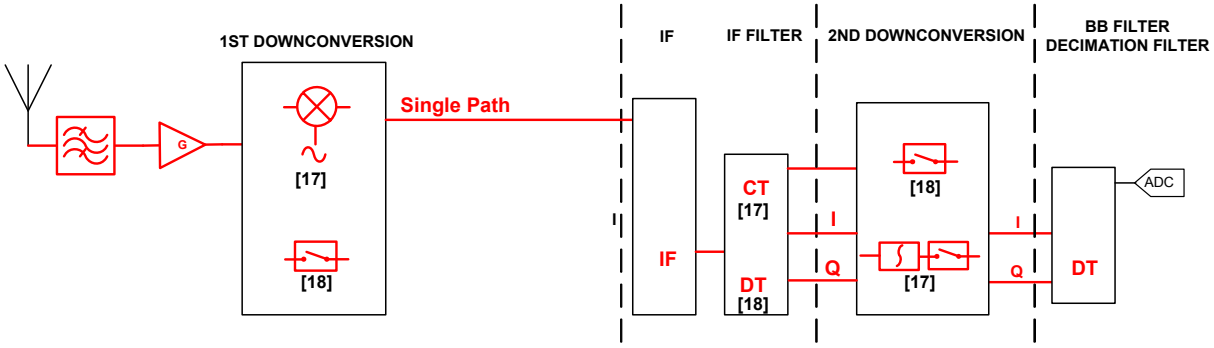


Figure 2-18 : – Down-conversion and filtering techniques for [17, 18]

In [18], the center frequency of the complex filter is equal to fc=fs/4. Through voltage sampling, the signal is down-converted to IF1=fc or IF1 close to fc. In [18], it has been chosen to have IF1=fc. In [18], two operating modes are observed: the first one implementing a high sampling frequency in order to reduce the S/H noise impact (2-14) and the second one applying half of the sampling frequency to observe the power savings. In Figure 2-19 and Figure 2-20 we illustrate the power budget for high and low sampling frequency modes and the power saving (20% less power consumption). The front-end filter rejects the first image frequency signal at f_{RF}-2·IF1. The decimation implements a second down-conversion. Where IF1=fc=fs/4 (which is the case for [18]), the signal is down-converted to zero-IF. In this case, the complex filter is used to separate I/Q signal. When fc=fs/4 the phase shift between I and Q paths transfer function at fc is $\pi/2$, therefore, quadrature sampling phase shift can be implemented using a single clock reference and several filtering paths. If IF2≠0, image rejection is implemented by using a

modified weaver structure ([22]). I/Q mismatch is avoided using single clock. The possible mismatches between the I/Q filter coefficients come from capacitance mismatch. The use of correct unit capacitances and dedicated layout techniques leads to very small mismatch. Therefore, it does not need compensation techniques which demand additional power consumption. In Chapter 5 we show the impact of the capacitance mismatches on a DT filter transfer function.

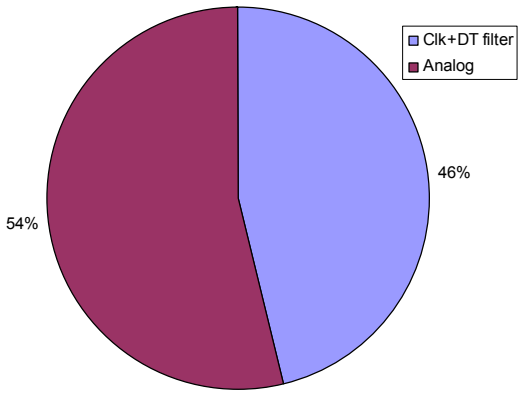


Figure 2-19 : – Power consumption Budget for [18], high fs mode.

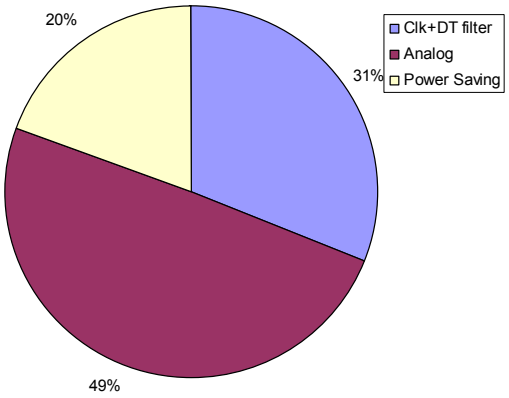


Figure 2-20 : – Power consumption Budget for [18], fs/2 mode.

In [17], the signal is first down-converted to an IF1 through classical mixer stage and bandpass filtered by a CT BAW filter. The front-end filter rejects the image frequency signal at $f_{im\_RF}=f_{RF}-2\cdot IF1$. Differently from [19], the various RF channels are down-converted to a single IF1. From this single IF1, there is no need to apply different sampling frequencies on blocks, which is the case for the architectures described in section 3.2. The CT filter at IF1 level can relax the required performances on the DT filter (see proposed architecture of Chapter 4). In [17] it was chosen to implement charge sampling and fs>IF1. When analyzing the double side spectrum, the IF falls on the negative side, which means the PSD of the sampled signal is mirrored at the positive side. The DT filter is frequency shifted to fc=-fs/4. In [17] a high IF1 is chosen, therefore, a high sampling frequency is needed, due to inherent charge sampling Sinc filter. The consequence is a high DT filter and the decimation orders on the implementation. During the sampling process, the signal shifts to a second intermediate frequency IF2, and differently from [18], we have IF2≠fc. The image signal at $f_{im\_IF1}=IF1+2\cdot IF2$ is rejected by the CT IF1 filter. In consequence, the decimation process down-converts the signal to a low-IF IF3. This choice is motivated to avoid the previously mentioned zero-IF drawbacks. The complex DT filter in this case is used to implement the image frequency rejection of $f_{im\_IF2}=IF2-2\cdot IF3$ at the DT filter level. This solution merges the complex filtering techniques (which relax I/Q mismatches) and avoids the drawbacks of zero-IF architectures.

Notice that the signal at IF2 is not placed at the center frequency of the complex DT filter, therefore, the filter transfer function is not optimized for the image frequency rejection. If it was the case, more selective filters such as complex IIR (see Chapter 5) should be applied. Finally, reducing sampling frequency through voltage sampling can lead to reduction of the frequency synthesis complexity thereby to the power consumption.

3.5 A Comparative Table Summarizing the DT architectures

Table 2-2 summarizes the discussed pros and cons of the various DT architectures from the SOA. In order to develop a quantitative comparison between these three architecture families, Chapter 4 is dedicated to derive the system level specifications for the focused BPS standards. A new architecture is presented, merging the positive points from each configuration and taking into account agility and power consumption.

<table>
<tr><th>Type</th><th>Ref</th><th colspan="3">Pros</th><th colspan="4">Cons</th></tr>
<tr><td rowspan="6">Direct sampling, DT filtering and decimation</td><td>[20]</td><td colspan="3">- low f_{OL}
- Simplified DT Filter
- Relaxed Front-End Linearity</td><td colspan="4">- Highly Sensitive to clock I/Q Mismatch
- 1/f - IIP_2 DC offset Sensitive</td></tr>
<tr><td>[6]</td><td rowspan="3">- Multiple RF Band Application</td><td>- Harmonic intermodulation Rejection</td><td rowspan="3">- Integration (no RF filter)</td><td colspan="2">$f_{OL}=8\cdot f_0$</td><td rowspan="4">- Sensitive to clock I/Q Mismatch</td><td rowspan="3">- High Front-End Linearity Needs</td></tr>
<tr><td>[4]</td><td>- High Performance DT Filter</td><td>- DT filter complexity</td><td rowspan="3">$f_{OL}=2\cdot f_0$</td></tr>
<tr><td>[2]</td><td colspan="2" rowspan="2">- Low-IF 1/f noise IIP_2 DC offset robust</td><td>- Multiple filtering decimation stages</td></tr>
<tr><td>[15]</td><td></td><td rowspan="2">- High Performance ADC Needs</td><td rowspan="2">- Sensitive to 1/f noise IIP_2 DC offset</td></tr>
<tr><td>[16]</td><td colspan="3">- Simplified DT filter
- Relaxed Front-End Linearity</td></tr>
<tr><td rowspan="2">RF/IF Bandpass Sampling</td><td>[14]</td><td colspan="3">- low f_{OL}
- Same DT filter + multiple decimation
- Low-IF</td><td colspan="4">- RF filter selectivity constraints
- Low selectivity on the Bi-quadratic filters
- Active DT filtering needs</td></tr>
<tr><td>[19]</td><td colspan="3">- Multiple RF + single fs_1
$-fs<f_{RF}$
- Relaxed Front-End Linearity Constraints</td><td colspan="4">- Wide Band IF filter Needs (fc/BW≈49%)
- Multiple RF filters Needs
- 1/f - IIP_2 DC offset Sensitive</td></tr>
<tr><td rowspan="2">RF/IF Bandpass Sampling with complex filtering</td><td>[17]</td><td rowspan="2">- No clock I/Q mismatch (complex DT filter)</td><td colspan="2">- Low-IF 1/f noise IIP_2 DC offset robust</td><td colspan="2" rowspan="2">- High f_{OL}
- High filter order needs</td><td colspan="2" rowspan="2">- 1/f noise IIP_2 DC offset Sensitive</td></tr>
<tr><td>[18]</td><td colspan="2">- $fs<f_{RF}$</td></tr>
</table>

Table 2-2 : Summary on the Pros and Cons

On the next section, we present the SOA of the basic blocks constituting various receivers architectures. Low power and ISM band oriented designs are preferred in this study. The derived performances will be compared with the ones specified on Chapter 4 for the ULP standards.

4 Discrete Time Receiver Base Blocks State of the Art

4.1 LNA

In a receiver chain, according to Friis formula [23], the contribution in terms of noise mainly comes from the first blocks in the reception front-end. This is explained by the fact that the signal is progressively amplified on the receiving path; therefore the generated noise of an intermediate block has less impact on the SNR degradation.

The first amplification stage in a receiver front-end is usually a *Low Noise Amplifier* (LNA), and in the case of charge sampling, it is realized using transconductance, defining a *Low Noise Transconductance Amplifier* (LNTA). Considering the total dynamic range at the front-end input, defined in Chapter 3. The LNA is adapted in terms of noise for the sensitivity and in terms of linearity considering the maximum input level. Along the overall dynamic range, power saving is possible by operating the LNA in different modes: high gain and low noise, or low gain and high linearity.

Usually, high performance and ULP LNAs are optimized for a given standard. On the frequency domain, this block performances are attained for a narrow band, mostly considering narrow band impedance matching. On the other hand, multi-standard approach motivates the use of wide band LNA. An intermediate solution consists in using multi-mode LNAs. An example is presented in [24] with reconfigurable narrow band impedance matching. The input or output impedance matching circuits can also be used as filters, relaxing linearity and filtering constraints. In [25] and [26], the output amplification stage implements a filtering function able to reject image signals.

Considering a given transmission environment, the LNA performances can be tuned in order to reduce power consumption, i.e. reducing over dimensioning for a given situation. For agile and low power receivers, various operational modes are interesting, addressing several bands or signal input power. In order to reduce the LNA surface technology scaling trends, inductors tend to be avoided. In the literature, an example of inductor-less LNA is found in [27]. Another advantage of inductor-less LNAs is the wideband impedance matching, which is desirable for RF multi-band applications. On the other hand, the constraints in terms of dynamic range increase the block power consumption. In order to compare the different studied LNA of the SOA, the figure of merit of [28] is applied. Since IIP3 and P are in Watts and f_{OP} in hertz, the unit for the FoM is hertz.

$$FoM_{LNA} = \frac{G \cdot IIP3 \cdot f_{OP}}{(NF-1) \cdot P} \tag{2-30}$$

Table 2-3 summarizes some low power LNAs performances, where f_{OP} stands for frequency of operation.

Ref-Year	Gain (dB)	IIP3(dBm)	NF(dB)	f_{OP}(GHz)	P(mW)	Tech.	FoM(dBHz)
[24]-2006	14.2	-6.5	2	2.14	6.8	0.25µm Si-Ge	95
[25]-2005	12	-3	1.8	2.4	0.9	0.18µm CMOS	106.2
[26]-2005	20.5	-5	1.5	5.5	12	0.18µm CMOS	106
[27]-2007	11	-7.2	4.8	2-9.6	19	0.13µm CMOS	87.8
[29]-2006	16.8	-11.2	3.9	1	0.1	0.18µm CMOS	104
[30]-2007	11.60	0.8	4.1	5.7	3.96	0.18µm CMOS	102
[31]-2005	9.2	-15	4.5	5	0.9	0.18µm CMOS	102.5
[32]-2005	13.6	7.2	4.6	1	0.26	0.18µm CMOS	113.9
[33]-2009	21	-18	6	2.4	1.6	0.18µm CMOS	90
[34]-2008	10	-17	4.76	2.4	0.4	65nm CMOS	87.8
[35]-2008	21	-10	5.2	2.4	0.63	0.18µm CMOS	103.2

Table 2-3 : The low power and/or wide band LNA SOA

Although the sub mW LNAs present relatively poor noise figure, the resulting performances are in accordance with ULP standards in which sensitivity specifications are relaxed. For wideband LNA, power consumption naturally increases with the linearity specification and the high operational bandwidth. In the case where only the ISM band is aimed at, the use of wideband LNA is to be avoided.

4.2 Frequency Transposition

4.2.1 Mixer

In this section, the principles of a mixer and the impact of its performances at system level are presented. Some performances of low power mixers are summarized in this section. A mixer block basically consists of a multiplication between two inputs. One is called the Local Oscillator lo(t), which defines the down-conversion, and the other is the signal itself $v_{in}(t)$. The Local Oscillator frequency varies to address all the targeted channels. The lo(t) is generated by a frequency synthesis , which are presented in 4.3. These can be *Phase-Locked Loop* (PLL) or *Delay-Locked Loop* (DLL). Considering lo(t) as a cosine wave centered at ω_0, the result of the mixing operation is given by:

$$s(t)\cdot\cos(\omega_0 t)\xleftrightarrow{\Im}\frac{1}{2}\left[S(\omega+\omega_0)+S(\omega-\omega_0)\right] \tag{2-31}$$

As observed, the mixing operates a down-conversion at IF1=(ω-ω_0) and an up-conversion at IF1'=(ω+ω_0). Now, let consider the case where two signals are localized at ω_1 and ω_2, and at the same distance from the ω_0. Figure 2-21 illustrates the mixing operation and the image aliasing.

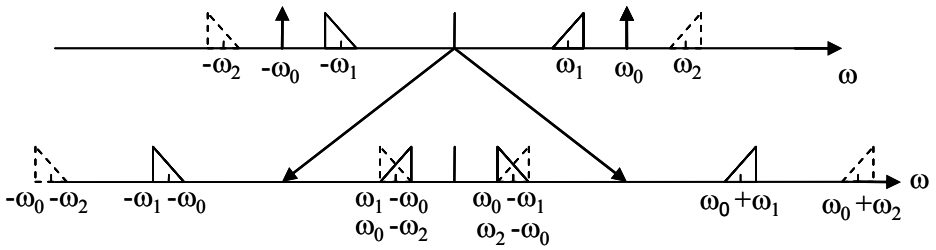


Figure 2-21 : The mixing operation and the image frequency aliasing

The choice of the Intermediate Frequency depends on several factors, most of them linked to the applied filtering techniques, but also on the lo(t) limitations. One constraint coming directly from the mixer is the 1/f flicker noise, for which particular attention is paid on the design process for low- and zero-IF applications [36]. The most common mixer architecture is the Gilbert cell [37]. The application of active mixer is mostly dictated by a need of reducing the LO amplitude on the mixer. It is important to notice that high gain and low noise figures can be achieved at the price of moderate non-linearity. In addition to the FoM presented for the LNA, the mixer FoM considers the LO input power. For weaker input oscillators, a considerable amount of power consumption can be saved on the frequency synthesis circuit. The passive mixer is not considered since performance improvement can be achieved while increasing the power consumption. The FoM is derived as follows and is analogous to Hz/W.

Table 2-4 summarizes mixers performances.

Ref-Year	Gain (dB)	IIP3(dBm)	NF_{SSB}(dB)	f_{OP}(GHz)	P_{LO}(dBm)	P(mW)	Tech.	FoM(dB Hz/W)
[36]-2005	-3	5	8.3	5	0	passive	0.18µm	
[38]-2006	10.9	-11.8	14.5	4.2	-2.6	0.2	0.18µm	144.2
[39]-2007	18	-4.4	9.1	2.4	0	0.5	0.18µm	131.9
[33]-2009	21	-18	6	2.4	0	1.6	0.18µm	120
[40]-2009	32	-14.5	8.5	2.4	-2	1	0.18µm	135.5
[41]-2009	12.7	-6	11.8	2.4	-14	0.38	90nm	137.2
[42]-2009	5.8	-6	13	5.2	-6	3.8	0.18µm	114.4

Table 2-4 : The low power and/or low 1/f noise or low LO power mixer SOA.

$$FoM_{MIXER} = \frac{G \cdot IIP3 \cdot f_{OP}}{(NF-1) \cdot P \cdot P_{LO}} \tag{2-32}$$

Observing the LNA and Mixer SOA, the CMOS 0.18µm technology seems the most commonly used for analog front-ends. For Zero-IF applications, the optimization of the 1/f flicker noise naturally increases the power consumption considering equal mixer performances. Very low power consumption are observed in [38] are [41], with performances still compliant with the application. In particular, while being low power consumption, the mixer in [41] is designed for low power LO input, which further relaxes the frequency synthesis buffers power consumption.

4.2.2 Sampler

We derived the transfer functions for voltage (section 2.2.1.1) and charge sampling (section 2.2.2.1), considering the sampling switches thermal noise. In this section, some sampling blocks from the SOA applied to BPS are presented. The BPS sampling process is either applied directly at the RF level [2, 15, 16, 43] or at IF one [44] [17]. Table 2-5 summarizes the BPS receivers. It can be observed from Table 2-5 that charge sampling has been preferred in recent implementations instead of voltage sampling. For the sampling circuits where the noise figure is low, pre-amplification or high sampling frequencies are applied. This conclusion can also be inferred from (2-17) and (2-29). To further reduce the KT/C noise, high capacitance values are applied, which naturally requires higher transconductance gains.

Ref-Year	Type	*f0*(MHz)	*fs*(MHz)	NF(dB)	Tech.
[14]-1996	Voltage	910	78	47	0.6µm Bi-CMOS
[44]-2003	Voltage	39	52	53	0.25µm CMOS
[45]-2003	Voltage	230	230	34	0.5µm CMOS
[46]-2003	Voltage	70	61.44	-	-
[2]-2004	Charge	2400	2400	15.9 (entire receiver)	130nm CMOS
[47]-2004	Voltage	2400	1072	22	0.18µm CMOS
[48]-2005	Charge	50	200	28	0.35µm BiCMOS
[15]-2005	Charge	900 / 1800	900 / 1800	17	90nm CMOS
[49]-2006	Charge	0	72 - 480	5 (entire receiver)	90nm CMOS
[17]-2006	Charge	921.6	1228.8	25 (simulation)	65nm CMOS
[16]-2008	Charge	2400 / 2700	2400 / 2700	4.8 (entire receiver)	65nm CMOS
[43]-2008	Charge	900	7200	18	65nm CMOS

Table 2-5 : The BPS process SOA.

4.3 Frequency Synthesis Blocks

Considering all the possible channels for the IEEE802.15.4 [50] and BT-LE [51], the minimum / common frequency step between two channels is 1MHz. In the case of RF BPS, the frequency shift is divided by the under-sampling ratio. Another important parameter is the synthesized frequency range. For low frequency synthesis where the entire RF band is covered, the consequence is an increase on the range fc/BW_{RF}, which directly impacts the VCO reconfigurability. The required performance for the frequency synthesis is strongly related to the frequency plan and the applied filtering functions in a given architecture. In this section we are interested in verifying whether reducing the frequency synthesis relaxes the power consumption or not. In order to compare the performance of the different PLL/DLL found in the literature, the following *Figure of Merit* (FoM) [28] is used:

$$FoM = \left(\frac{f_0}{\Delta f}\right)^2 \cdot \frac{1}{\left(L(\Delta f)\cdot P\right)} \tag{2-33}$$

where: f_0 is the VCO center frequency, Δf is the distance from f_0 where the phase noise is measured, $L(\Delta f)$ is the phase noise @ $f_0+\Delta f$, and P is the power consumption of the VCO. Table

2-6 summarizes the performances on the frequency synthesis. This FoM is defined for VCOs. In some references is only given the total PLL / DLL power consumption, therefore we consider both power data to calculate the PLL / DLL referred FoM and/or the VCO referred FoM. Considering the latest low power development on the frequency synthesis, the objective is to highlight the trend of the FoM as a function of the frequency. Figure 2-21 summarizes the derived FoMs. As observed, FoM of LC-VCOs tends to keep the FoM considering lower frequencies such as 641MHz [52], 698MHz [53] [52], compared to those around 2GHz [54, 55]. This constant FoM over the frequency is related to the inductors and capacitors quality factors which do not particularly vary over the frequency. This result shows that it is not particularly interesting to have higher generated frequencies to increase the FoM. While ring oscillators offer better integration and frequency range, they offer worse FoM [56, 57]. Another important aspect is that the output buffer power consumption is not considered, power consumption which is expected to increase at higher frequencies. The power consumption on the clock tree and the synthesis may represent up to 40% of the total receiver power consumption (Figure 2-15 and Figure 2-16).

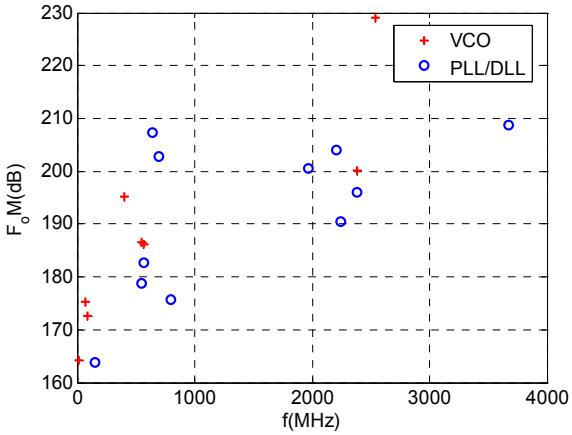


Figure 2-22 : VCO & PLL/DLL FoM SOA

Ref-Year	Type	f_C (MHz)	L(Δf) (dBc/Hz)	Δf (MHz)	P_{VCO} (mW)	P (mW)	Tech (nm)	FoM VCO (dB)	FoM tot (dB)
[58]-2006	Fract. PLL- Poly LC-VCO	400	-120	1	1.2	-	180	195	-
[59]-2007	Fract-PLL	1850	-109	1	-	14	130		190.5
[60]-2007	BAW-VCO	2514	-93	0.01	1.6	-	180	229.1	-
[60]-2007	IF-CCO	70	-104	1	0.36	-	180	175.3	-
[56]-2007	Ring-VCO PLL	568	-91	1	0.1	0.225	130	186.1	182.6
[61]-2008	Ring Fract- PLL	3670	-132.9	3	-	39	130	-	208.7
[62]-2008	Ring VCO PLL	305	-97.9	1	-	6	180	-	163.8

[53]-2008	LC VCO PLL	667	-132.5	1.45	-	21.6	180	-	202.9
[63]-2008	Ring PLL/DLL	800	-115	6	-	15	90	-	175.7
[64]-2008	Relaxation Oscillator	6.5	-110	1	0.09	-	65	164.2	-
[65]-2009	DCO-BAW ref	2383	-104	1	1.35	3.6	180	200.2	196
[65]-2009	IF-CCO	84.9	-104	1	-	0.98	180nm	172.7	-
[57]-2009	Ring VCO PLL	485	-95	1	0.21	1.25	130nm	186.6	178.8
[54]-2009	LC-VCO PLL	2210	-141.9	20	-	7.56	180	-	204
[55]-2009	LC-VCO ΔΣ-PLL	1990	-128	3.5	-	17.2	180	-	200.6
[52]-2009	LC-VCO	645	-122	1	-	1.2	130	-	207.4

Table 2-6 : The frequency synthesis SOA.

* The phase noise measurements are given for a frequency different from fc.

4.4 Filtering Blocks

Figure 2-23 classifies the various filtering techniques and their applications on RF DT systems. Therefore, in this study, the base band CT based filters, either RC or gm-C base band, are not considered. The presented filtering techniques can be found on the architectures presented in section 3, and can be further dedicated to reduce the receiver power consumption or to give a certain degree of reconfiguration on the receivers. While CT passive filters are often off-chip and present fixed mask, they also relax dynamic range and phase noise specifications for the consequent blocks. If a passive block implement channel selection, great power saving is observed on the base band filters and ADCs. DT filters can be reconfigurable just by changing the capacitance array, therefore the coefficients. Another advantage is that the frequency response follows the sampling frequency, therefore several channels can be addressed while the transfer function adapts dynamically. DT filters have the drawback of presenting losses and high noise (KT/C), while the overall clock power consumption can increase for high order filters.

In Figure 2-23 we observe a general context of the filtering challenges in a receiver. The filtering mask strongly depends on the architecture type and the chosen frequency plan. Different needs appear depending on such choices: image filtering, anti-aliasing. For techniques which are applied for the same filtering application, we present a comparison in terms of integration, reconfiguration and power consumption aspects.

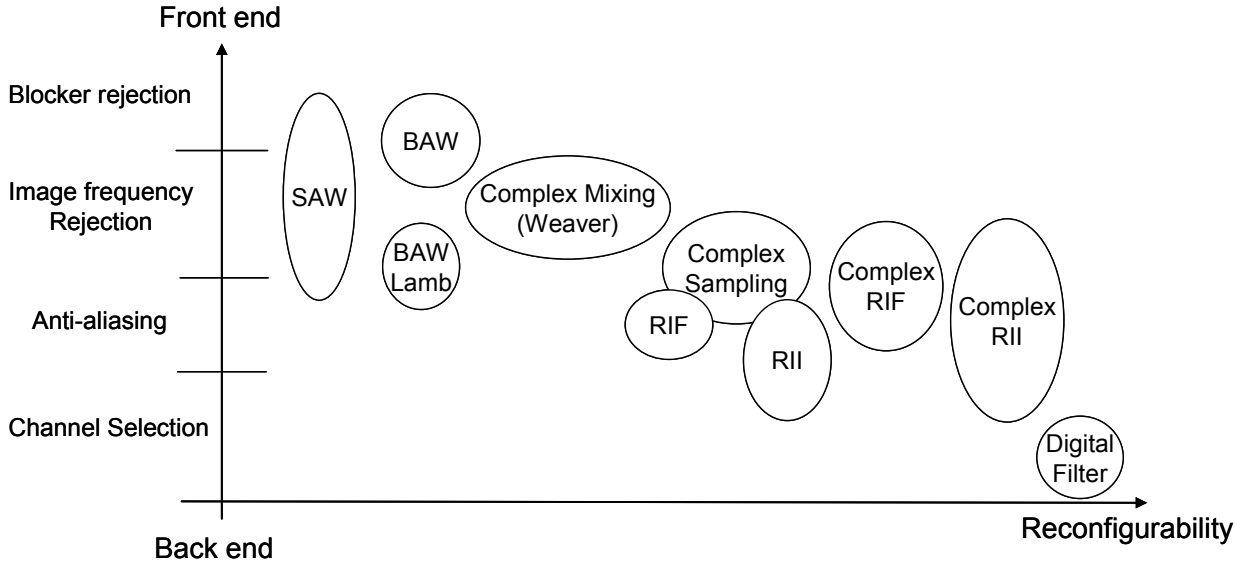


Figure 2-23 : Filtering techniques and applications on the receiver signal flow

The filter design process presents the following stages:

- Mask definition
- Filter order, coefficients, and prototype filter
- Possible down-conversion (decimation filters)
- Coefficients implementation: Choice of technology, network and sizing.

In this section we present a brief SOA of the filtering techniques and their pros and cons.

4.4.1 RF filter

In a telecommunications context where the available spectrum is progressively crowded, the standards aim at occupying narrower bandwidths. In this context, the RF front-end filters need to present strong rejections at very close to the carrier frequencies. In full-Duplex systems, such as PCS standard, the uplink and downlink bands are very close to each other. In cellular standards, for which high dynamic range is mandatory, very stringent rejections are required.

The signal of interest can be blocked by the RX non linearity and the presence of strong out-of-band signals, called blockers. The RF front-end filter rejection is mainly defined from the blockers profile specifications and on the receiver linearity. The LNA IIP3 is the major constraint when low RF rejection is present. The most popular technology implementing front-end RF filters is the SAW technology, which employs the piezoelectricity principle [66]. The application of an electrical field on this structure induces mechanical compression which changes the electrical field on the structures. This interaction is optimal for a given frequency, which characterizes the resonance frequency. A resonator is the basic block to design filters. In SAW components, the mechanical waves are concentrated on the device's surface. Possible resonance frequencies vary from fc=30MHz to 2.7GHz. This type of filter is not adapted to integration on monolithic IC, which is a strong benefit in order to reduce losses and implementation costs. A good candidate to substitute SAW filters is the BAW filters [67]. In this case, the acoustic wave is longitudinal oriented in a piezoelectric layer sandwiched by two electrodes. The piezoelectric layer thickness defines the resonance frequency. Applicable center frequencies vary from

fc=800MHz to 10GHz [68]. The BAW technology is becoming more reliable and can substitute classical SAW filter. The main advantages are: smaller surfaces and well-adapted for co-integration with CMOS processes.

The multi-band aspect can be addressed by reconfigurable narrow band LNA and RF filters. In [69], a center frequency reconfiguration technique for BAW technology filters is proposed. Since the center frequency of such filters is dependent on the piezoelectric layer thickness, the technique is based on changing this thickness through the application of mechanical switches, which connects a load layer to the resonator. An example of bandwidth reconfiguration is presented in [70], on BAW technology. The filter bandwidth is dependent on a technological parameter called coupling coefficient. When added in series with a resonator, an inductor increases the bandwidth. Switched inductors are applied to change the filter BW to the targeted one.

4.4.2 Passive IF filter

When fixed-IF is applied for all channels, the IF filter can implement much more selective filtering which brings several advantages. First, adjacent interferers can be rejected in order to relax linearity constraints on the successive blocks. In classical heterodyne receivers, the IF filter also relaxes the constraints on the base band filter and on the ADC dynamic range. Ideally, an IF filter should implement the channel selection, excluding the need for base band filters. In the case of a BPS technique, the IF filter is used as an anti-aliasing filter as well. In this case, an ideal IF filtering can suppress the need of DT filter and decimation stages (directly sampling at the ADC sampling frequency). As it was presented in section 2, the aliasing phenomenon happens at multiples of the sampling frequency. The aliasing factor depends on the in-band/out-band noise ratio (Δn of Figure 2-8). In order to implement low BW filters, the IF frequency is relatively low. Indeed, on the implementation level there is a technological parameter which defines the relative bandwidth in BW/fc which is a limiting factor. For BAW and SAW technologies, this parameter is called the coupling coefficient. For LC filters, the quality factor defines the relative BW.

When a second low IF2 is applied, the IF filter can be used to implement the image rejection at IF-2·IF2. When BPS architectures are applied, the IF1 also implements anti-aliasing rejection. Another concern on the IF filter implementation is its co-integration with CMOS technologies [71]. As presented on the previous sections, BAW filters are limited above 800MHz, and selective IF filters are difficult to obtain in this range. On the other hand, SAW technologies are still used for IF filtering.

In order to merge the integration advantage of BAW filters and yet address lower IF, LWR filters is a strong candidate technology. These filters can achieve very selective filtering performance (elliptic function) at center frequencies below 500MHz [72]. Another advantage of LWR technologies is the possibility of addressing high characteristic impedances, thus reducing the constraints on the current driving the filter. As for BAW resonators, the acoustic wave is found on the resonator volume, but in this implementation, it propagates on the lateral orientation. Different propagation harmonic modes can be applied. Since the basic block is still the resonator, examples of filters implemented in LWR technologies [73] also contain the basic

electrical coupling networks (ladder and lattice), or mechanical coupling (stacked in coupled resonators).

In the literature, the SAW filters have been used for IF filtering in [74] for *Digital Terrestrial Television* (DTTV) applications, and some other applications such as CDMA IF filtering [75] can be found in the literature. Table 2-7 summarizes the SOA of the IF passive filtering techniques. The results from Table 2-7 show that the LWR technology still needs considerable evolution in order to achieve SAW filters performances. On the other hand, the high achievable impedance characteristics still motivates the research on such technologies.

Tech.	Type	fc (MHz)	IL(dB)	Rej. @2MHz @3MHz @5MHz	BW/fc (%)	Z_0(KΩ)	L (μm) × L (μm)
LWR	Stacked[73]	156,5 233 160,1 164,3	-7.3 -5.6 -3.5 -9.3	-	0.47 0.28 0.25 0.67	1 1 1 1	52 × 323 35 × 323 52 × 323 52 × 323
	Coupled Res. [73]	160	-22	-	4.4	1.25	204 × 323
SAW	DTTV [74]	56	-	45 45 45	5.36	-	-
	CDMA IF [75]	380	-5.8	5.8 30 53	1.21	-	3200 x 5000

Table 2-7 : LWR and SAW IF filters summary

4.4.3 Analog Discrete Time Filtering

As presented in section 3, the analog DT filtering is placed between the sampling circuits and the ADC. Recent interest is paid on such techniques since they are adapted to the miniaturization/integration trends, and offer some degree of reconfigurability. Details on DT filtering theory are presented in Chapter 5. In this chapter we present some implementations proposed in the literature as well as the basic characteristics of the filtering function.

4.4.4 Finite Impulse Response (FIR)

IF BPS architectures are shown in [17, 44, 46, 49]. An implementation of a four-tap filter which represents a finite impulse response is presented in [76] (Figure 2-24). From phases $\phi 1$ to $\phi 4$, four samples are obtained in the capacitors from C1 to C4. Each one of the capacitors is connected to a transconductance amplifier providing charge sampling (section 2.2.2). The sum of the currents represents the sum of coefficients. A reset phase is set when $\phi 0$ goes to zero, defining a FIR filter. When the capacitor sizes are equal, the filtering function is a Sinc one, where the zero transmissions are at $n \cdot fs/4$ (n=1,2,3), for anti-aliasing before decimation. Since one sample is considered at the output for each four input samples, decimation by 4 is implemented. From Figure 2-24 (a) we observe two possible reconfiguration techniques, the first

is by implementing an array of capacitors in order to change the equivalent capacitance connected on phases ϕ1 to ϕ4, the second is to change the transconductance gm_0 connected to each filter capacitor, on the decimation phase.

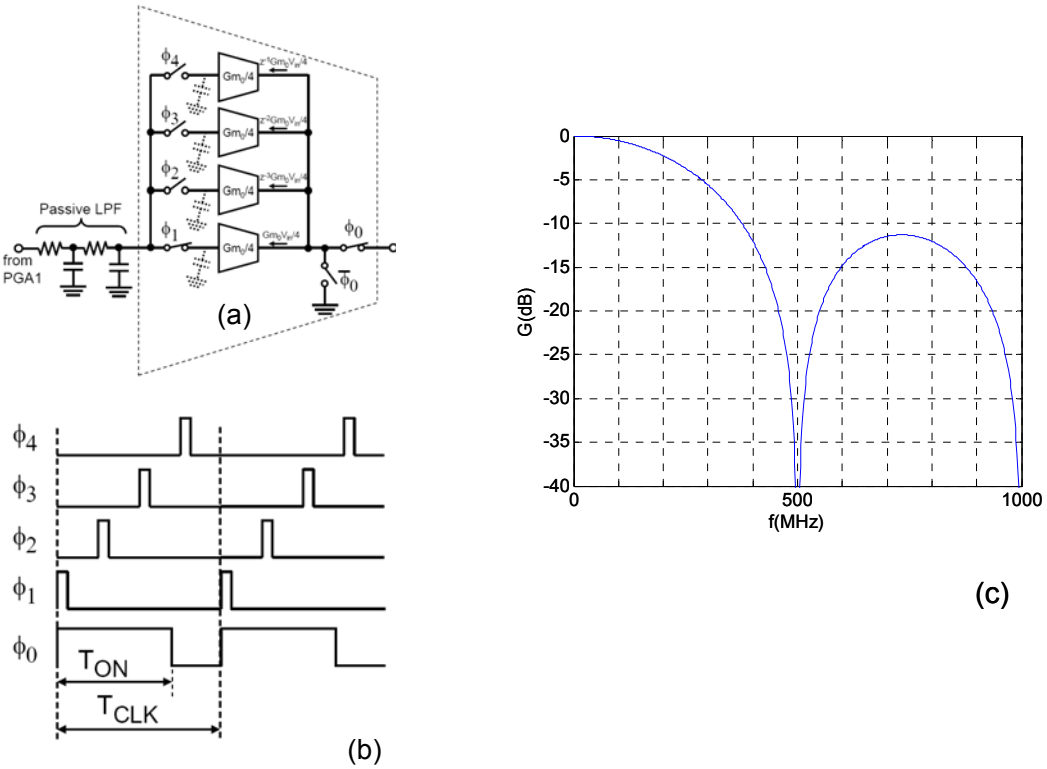


Figure 2-24 : FIR filter from [76]. (a) Schematics, (b) clock tree, (c) frequency response

A filtering reconfiguration technique is proposed in [77] (Figure 2-25). In this topology, the capacitors C1 to Cn, as presented in Figure 2-24, are substituted by a sequence of capacitances containing "m" capacitors. The capacitance ratios follow the power of 2, in order to define different values $Ck=2^k \cdot Cu$, where Cu is the unit capacitance. When "m" capacitances are used, 2^m different coefficients are possible. The drawback of this topology comes from the output switches, which number is multiplied by "m". Each output switch contains parasitic capacitances drawing an amount of the sampled charge, which leads to charge variations.

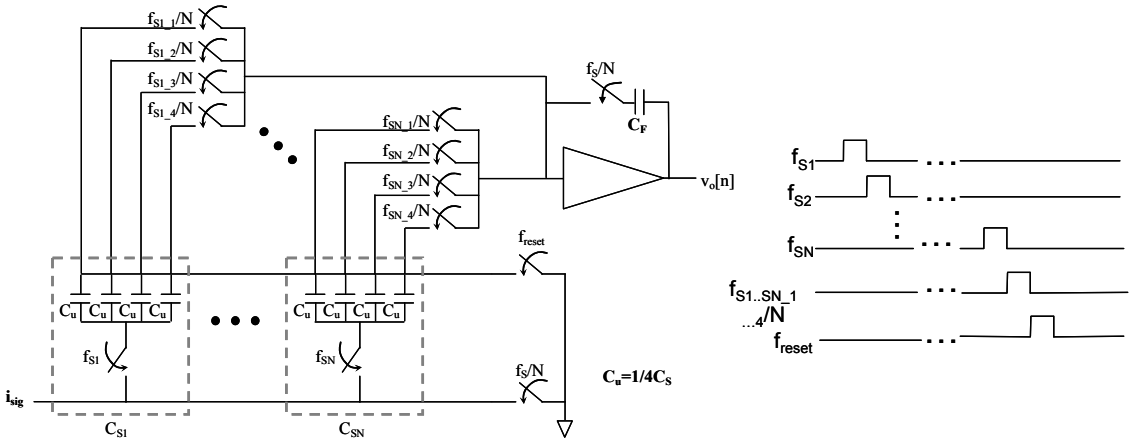


Figure 2-25 : Reconfigurable FIR filter

Another technique for coefficient reconfiguration is considered at the charge sampling level, where the output voltage is dependent on the total charged period (equations (2-21) and (2-22)) and on the transconductance gain ([78]). During the charge sampling, the charge can be accumulated over a single capacitance using an *Operational Transconductance Amplifier* (OTA). The output samples are controlled by $\phi 2$ and the different charge integration periods can be controlled by $\phi 1$. Another reconfiguration strategy is to apply different "gm" per sample, changing therefore the filter coefficients ([17]).

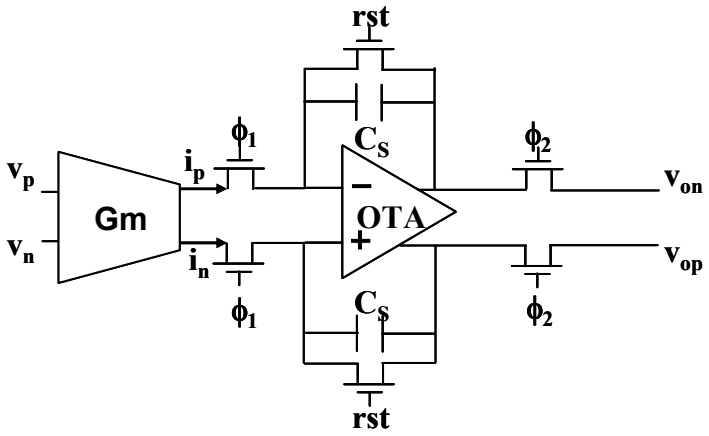


Figure 2-26 : Sampling network applying an OTA and feed-back capacitors

4.4.5 Infinite Impulse Response (IIR) filter

The main difference of IIR filters compared to FIR is that it depends not only on a certain number of input samples, but also on a certain number of the output ones. The IIR filter theory and its implementation are detailed in Chapter 5, but in practical terms, the reset phase can be suppressed in an IIR filter. An implementation illustration of such filters is proposed in [79] (Figure 2-27). The sampling is applied in the charge domain, but the idea of the rotating capacitances can also be used on the voltage sampling technique.

In a first stage, the capacitors C_H and C_{R1} are connected to the input and N samples are charged into them. This first stage represents a FIR Sinc filter with zeros at n·fs/N (n=1,2,3,..N-1) (Figure 2-29). After N cycles, C_H contains a_1 of the total sampled charge, and C_R contains the rest of the charge 1-a_1. When SAZ goes to "1" and SA to "0", C_{R2} receives a part of the last sample that was kept in C_H, $_H$ stands for History Capacitance. This interaction implements an IIR since C_H contained a portion of the last output charge filter. It generates poles at n·fs/N (n=0,1,2,3,..N-1) (Figure 2-29). The combination of the FIR and IIR transfer functions gives the frequency response of Figure 2-29. The filter gain depends on the number of samples accumulation and on the feedback coefficient implemented between C_H and C_R. In Figure 2-29 and Figure 2-30 we illustrate the normalized gain frequency response. Various bandwidths and gains can be implemented by changing the C_H value (array of capacitances). On the other hand the filter notches are fixed to n·fs/N. This filtering technique is used in [2] and [15]. This filter merges the advantage from the FIR stage notches for anti aliasing, and the selectivity achieved by the IIR stage, which can be used as channel selection.

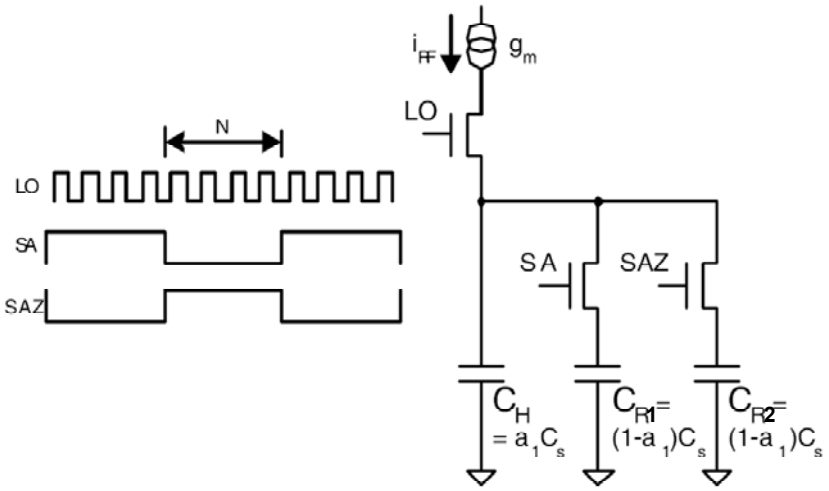


Figure 2-27 : IIR filtering through rotational capacitors.

In order to improve the filter rejection, the IIR transfer function was added to a Sinc² FIR transfer function ([49]). Figure 2-28 illustrates the DT filer implementation on [49] :

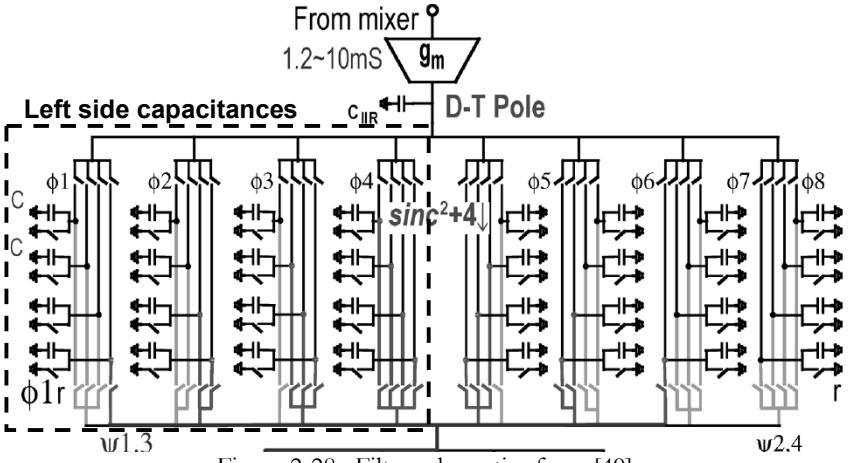


Figure 2-28 : Filter schematics from [49]

As presented in [79], the IIR transfer function is implemented thanks to an « history » capacitor, (C_{IIR} in Figure 2-28). The rotating capacitance presented in [79] is replaced in this case by the network of capacitors connected on the charge process on the phases ϕ1 to ϕ8. The Sinc² transfer function requires 8 coefficients with a decimation order of 4. The inverse Fourier Transform of the Sinc² function is a triangle, which gives the coefficient definition for the Sinc² filter. This network implements the following sequence coefficients: [1 2 3 4 3 2 1 0]. From ϕ1 to ϕ4, the capacitances of the left hand side are charged. To generate the coefficients, one capacitor from ϕ1, two from ϕ2 and so on, are discharged. From the right hand side capacitors the coefficient continues (3 2 1 0). From ϕ5 to ϕ8 the right side capacitors are charged. From the last output, three capacitors from ϕ1, two from ϕ2 and so on, were not discharged and represent the coefficients for this stage (3 2 1 0). The coefficients (1 2 3 4) are implemented with the right side capacitances. The ratio between C_{IIR} and the sum of capacitances of a branch ϕn, implements the IIR pole, as it is defined between C_H and C_R on Figure 2-27. Figure 2-30 summarizes the FIR, IIR and composed filter frequency response.

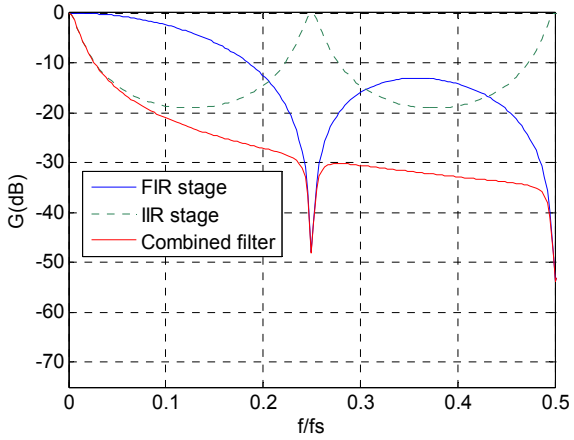


Figure 2-29 : The filter of [79] frequency response N=4

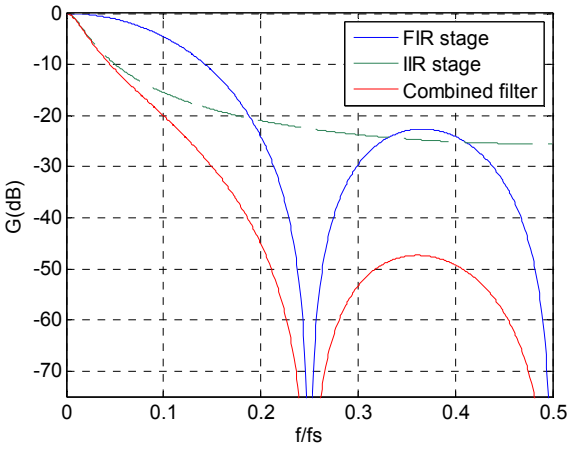


Figure 2-30 : The filter of [49] frequency response

4.5 Analog to Digital Converter

In this section we study the SOA for the ADC paying particular attention to sub mW ADCs. ADCs performance comparison are based on the following FoM [80] et [81] :

$$F = \frac{2^{nbeff} \, fs}{P_{ADC}} \tag{2-34}$$

where nbeff is the effective number of bits, fs is the sampling frequency, and P_{ADC} the ADC's power consumption.

For low power applications, continuous research is being carried out in order to optimize FoM, where improvements can be observed for new topologies and technologies. In the context of *Software Defined Radio* (SDR) where high performances are required at the cost of power consumption, the FoM is no more relevant ([80]).

Figure 2-31 shows how the FoM increases over the years with the introduction of new technologies. As observed, some ADC really stands out from the interpolation for the predicted FoM. The objective is to verify if such ADCs are low power oriented or performance oriented. From [82], a wide ADC performance survey is proposed, from 1997 to 2010. Details on the ADC performances can be found and compared. To fit in our application, we focused on the ADCs which power consumptions are around P_{ADC}=1mW and to calculate the average FoM on low power ADCs. Table 2-8 summarizes the ADC's presented in the lasts VLSI and ISSCC conferences whose power consumption is around P_{ADC}=1mW. The average FoM is FoM_{RMS}=2.3x10^{13}.

Ref-Year	Architecture	Tech.(nm)	SNDR(dB)	f_s(MHz)	NF_{eq}(dB)	P(mW)	FOM
[83]-2008	Pipeline	90	47.7	50	56.3	1.44	6,75E+12
[84]-2008	Pipeline	65	54.3	26	52.5	5.51	1,96E+12
[85]-2008	SAR, TI	65	28.4	250	68.6	1.2	4,39E+12
[86]-2009	SAR	130	52	50	49	0.92	3,46E+13
[87]-2009	SAR	90	32	50	72	0.24	6,64E+12

[88]-2009	SAR	130	62.4	11	48.2	3.6	3,23E+12
[89]-2009	Binary Search	65	27	800	65	1.97	7,28E+12
[90]-2010	SAR	180	60.3	10	50.7	0.98	8,45E+13
[91]-2010	SAR	90	54.1	150	45.1	1.53	3,97E+13
[92]-2010	Pipeline, Folding, TI	40	31	2200	56.4	2.6	2,43E+13
[93]-2010	SAR	130	67.1	45	37.4	3	2,70E+13
[94]-2010	Pipeline, SAR	65	52.5	40	52.5	1.2	1,12E+13
[95]-2010	SAR	90	48.4	10.2	62.5	0.07	3,13E+13
[96]-2010	SAR	65	56	100	45	1.13	4,47E+13

Table 2-8 : The low power ADC SOA

SAR stands for *Successive Approximation Register*
TI stands for *Time Interleaved*

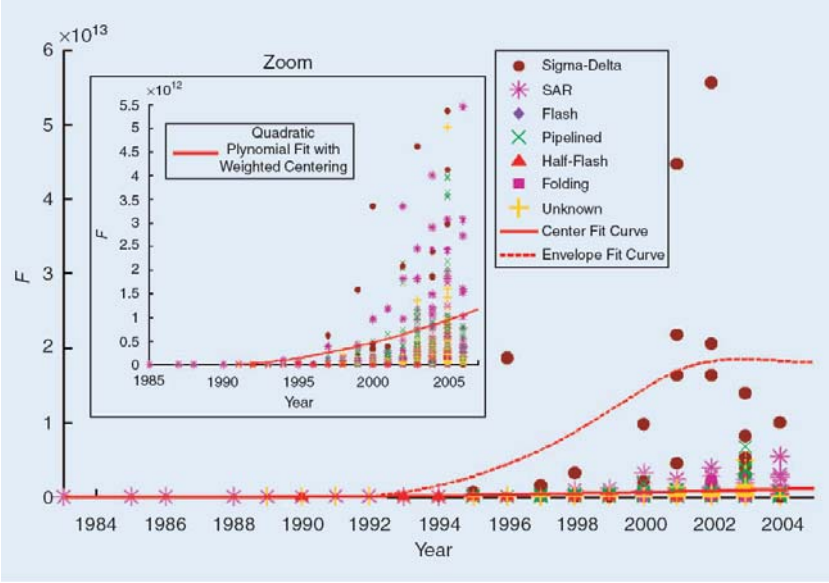


Figure 2-31 : FOM evolution over the years ([80])

Although most of the latest ADCs are implemented in 90nm and 65nm, the best FoM are attained for 130nm and 180nm technologies, like for low power LNAs (Table 2-3) and mixers (Table 2-4)). Later in Chapter 4 we will observe that the proposed architecture needs an over sampled ADC. Although ΔΣ converters are dedicated for over sampled applications, they are dedicated to applications where the resolution and the over sampling ratio are higher than the specified ones in Chapter 4. We observe from Table 2-8 that most of the under 1mW ADCs are pipeline and SAR topologies, which are not usually applied in over sampled ADCs, but considering the proposed frequency plan and ADCs specifications in Chapter 4, they fit to the application.

5 Conclusion

From the context of low power consumption and *Discrete Time* (DT) oriented architectures, which are adapted to multi-standard applications and follows the technological evolution towards integration/down scaling, the BPS technique is presented as a solution to

reduce frequency synthesis constraints on receivers, to implement down-conversion and the *Continuous Time* (CT) to DT conversion. From the presented definitions of the BPS and the basics on the voltage and charge sampling, we observe that applying charge sampling is not adapted to high under-sampling ratios. We also observe that the voltage sampling RC time constant is less constraining in a BPS process than in a Nyquist sampling process.

From the SOA, we observe three main families of DT architectures, the first presents high sampling frequencies (mainly due to the fact that charge sampling is applied), high order DT filter and several decimation stages. They are oriented for integration and reconfigurability but they suffer from high power consumption. The second reduces the frequency synthesis while applying voltage sampling. On both families the complex mixing is a strong drawback in terms of I/Q mismatch. The third family presents the complex DT filtering to pass the problem from I/Q mismatch but still needs high filter and decimation orders from a non optimized frequency plan and complex DT filter design (where the used of IIR filter is impossible).

On the next chapters, the data obtained in this SOA study will be used as reference for comparing the blocks specifications defined on the architecture dimensioning in terms of power consumption. The typical performances and FoM are orients the architecture definition and design. As observed, the DT filtering techniques and the frequency synthesis circuits represent the major power consumption on DT architectures. The clock tree and the synthesis can represent from 30% to 40% of a DT RX power consumption. With careful frequency plan and filtering strategies, theses blocks power efficiency can be significantly improved. For that goal, the DT filtering and the phase noise in BPS process will be analyzed in detail in Chapter 5 and Chapter 6.

Motivated by the new challenges on the system level design considering the BPS, the next chapter is dedicated to define a new system level design methodology and simulation tools based on BPS and DT architectures. In the objective to merge the positive points from each architecture family and to improve beyond the limitations presented, we present a quantitative comparison on Chapter 4. From this study, a new architecture is also proposed and analyzed applying the system level methodology and simulation tool.

Chapter 3 : System Level Modeling and Design Methodology

1 Introduction

Classical system level design flow starts from a spread sheet calculation. System level parameters are applied block after block in order to calculate the receiver equivalent performance (Gain, Noise Figure and IIP3) [97]. This high level approach leads to macro parameters specifications considering a limited number of imperfections. Although this technique has been widely used, with the expansion of the telecommunications especially in terms of miniaturization, cost effectiveness and low power consumption, new system level constraints have appeared. Not only the standards specifications must be considered, but also other constraints like agility and discrete time multi-standard receiver in the scope of ultra low power consumption. Classical system design flows are often limited to over-specifying front-end blocks, which naturally kill the optimization in terms of power consumption. With precise modeling, the distribution of system specifications over the whole receiver chain must be defined considering the least possible margin. The contribution of each block is related to the required performance and of course its implementation limitations.

The first part of the chapter is dedicated to define the standards framework. The Physical layer specifications for the BT-LE and IEEE802.15.4 standards are presented in section 2. In section 3 we present an iterative system design method which translates a given performance distribution into individual block specifications for a given standard and architecture. In [98], it was shown the importance of using a method to quickly converge to the specifications when a block performance is changed. We propose two main improvements in our methodology: an automatic method suited to BPS receivers and the possibility to apply arbitrary SNDR degradation distribution.

On the system level simulation, most tools and practices are dedicated to the digital base-band rather than to the RF section. Data flow simulation is applied considering the physical layer equivalent performance (G, NF, IIP3) referred to base band, where the base band algorithms are evaluated in order to derive BER x SNDR curves. This approach contains low detailed model from the physical layer. Between these two approaches there is a gap where some key imperfections to be considered are neglected. For that matter, studies have been made with frequency domain based simulators (Fasyle, SystemVue). More detailed RF modeling solutions are considering time domain behavioral modeling, defined by the blocks transfer function, which is close to circuit level transient simulation. These models can be integrated with circuit level simulation through programming languages such as Verilog-A and VHDL-AMS. This approach can be referred to the base band, which is the case for the complex envelope modeling ([99]). These techniques can be integrated with the base band algorithms were a more in depth analysis of the system is implemented. The major drawback is the simulation time and agility, where the idea is to fine tune block specifications and display phenomena that were not identified on the first system level approach (spread sheet calculation).

As new architectures have been developed, new techniques, such as ultra wide band or the BPS processes push concepts of signal processing and change the system level approach. We

showed in CHAPTER 2 that interferers, blockers and non-linear products, can fold into the band of interest on the BPS process. The wideband noise is also aliased inside the Nyquist band. The BPS in particular is a technique where a wide spectrum representation is necessary to correctly model the system and to define the SNR. In section 4 is presented a system simulation tool developed in MATLAB in which the analysis is focused on the frequency domain. The local SNDR is the figure of merit to evaluate and validate a given architecture. Calculations are implemented either in time domain or frequency domain, to increase calculation speed.

2 Detailed Framework on the IEEE802.15.4 and Bluetooth Low Energy PHY-Layer

The standards IEEE802.15.4 [50] and BT-LE [100] were created in a context of short distances and low data rate networks. Three different types of networks are identified: WPAN, WBAN and WS&AN. The historical evolution of these networks is presented in the INTRODUCTION and in this section we summarize the general specifications for the PHY layer of both standards. These specifications are embedded in the tool presented in this chapter in order to develop the comparison between the DT architectures in CHAPTER 4.

2.1 General Aspects

2.1.1 IEEE802.15.4

The IEEE802.15.4 was created as an RF communication link for Automation / Control in a Wireless Sensor Network. It relies on one MAC layer, but three PHY operation modes, one wideband in the *Industrial Scientific and Medical* (ISM) band at 2.4GHz-2.48GHz, two other narrowband ones in the 868MHz & 915Mhz ISM band. The Worldwide ability of the 2.4 GHz band and the fact that it is also the band for the BT-LE standard makes this band the most interesting one, and surely the most popular to be employed. Table 3-1 summarizes the general aspects of the IEEE802.15.4 - 2.4GHz PHY layer ([51]):

Parameter	***Specifications***
Channel Center Frequencies (MHz)	$2405+5\cdot(n-11)\quad n \in (11...26)$
Channel Bandwidth (-30dBc)	2.45MHz
Data Rate	Symbol=62.5 kbps
	Bit=250 kbps
	Chip=2 Mcps
Modulation Type	O-QPSK - Half sine pulse shaping filter (AMSK)
Multiple Access Mode	In-channel DSSS + CSMA-CA

Table 3-1 : General aspects of the IEEE802.15.4 - 2.4GHz PHY layer

The IEEE802.15.4 modulation scheme is based on the *Direct Sequence Spread Spectrum* (DSSS) technique which by adding redundancy increases multiple path / noise robustness. There are 16 different chip sequences; each chip is labeled by a 4-bit symbol. Therefore, each 4 bits on

the data-flow constitute an input symbol for the spreading function, leading to the chip sequence. Each chip sequence is made of 32 chips, which typifies the spectrum spreading function. Therefore the data rate is 8 times slower than the chip rate (32 chips, 4 bits, 1 symbol). The symbol-to-chip mapping is defined on ([51]). The Chip sequence is *Offset Quadrature Frequency Shift Keying* (O-QPSK) modulated. The I and Q paths are shifted by a delay, which is equal to the Chip Period Tc (Figure 3-1). The offset is employed in order to have less amplitude variation on the modulated signal compared to its non-offset counterpart. In consequence, better *Peak-to-Average Ratio* (PAPR) is achieved, which allows to operate the *Power Amplifiers* (PA) in non-linear regions.

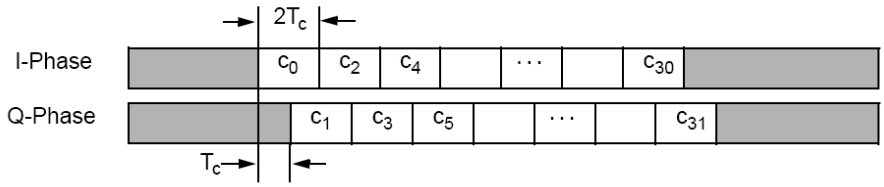


Figure 3-1 : O-QPSK chip offset.

The defined Chip sequence is therefore half sine pulse shaped (3-1):

$$p(t)=\begin{cases}\sin\left(\pi\dfrac{t}{2T_C}\right), & 0\le t\le 2T_C\\ 0, & otherwise\end{cases} \tag{3-1}$$

Applying the spreading function and the O-QPSK modulation for the "0" sequence, we obtain the sequence of Figure 3-2:

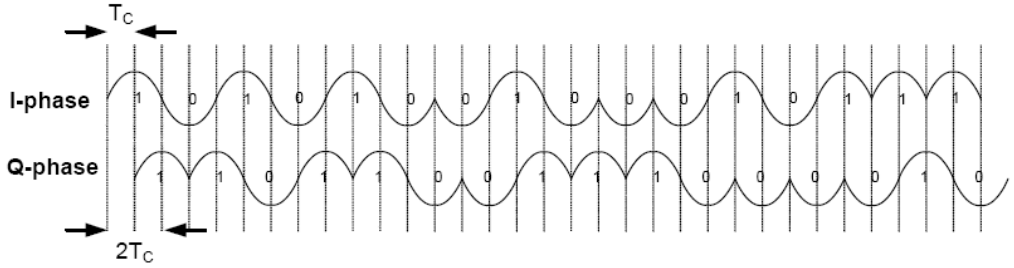


Figure 3-2 : Sample baseband chip sequence with pulse shaping for the "0" sequence.

2.1.2 Bluetooth Low Energy

Table 3-2 summarizes the general aspects on the BT-LE - PHY layer ([100]):

Parameter	***Specifications***
Channel Center Frequencies (MHz)	2402+2·n n ∈ (0...39)
Channel Bandwidth BWch (-30dBc)	1.25 MHz
Bit rate Rb	1 Mbps
Modulation Type	GFSK BT=0.5 Modulation Index m, m ∈ (0.45 … 0.55)
Multiple Access Mode	CSMA - FDMA - Frequency Hopping

Table 3-2 : General aspects on the Bluetooth Low Energy

The occupied band for the BT-LE signal is higher than compared to the classical Bluetooth specifications, which leads to lower spectral efficiency but better BER x Eb/N_0 performance.

2.2 Sensitivity

The *Bit Error Rate* (BER) is one of the main specifications when considering the Quality of Service (QoS) defined for a given standard. Also, the *Signal- to-Noise Ratio* (SNR) is the ratio between the power of the signal of interest and the noise inside the bandwidth occupied by this signal. In order to evaluate the performance of different modulation schemes, the concept of *Energy-per-Bit-to-Noise Density* (Eb/N0) is used and is a normalized SNR, also known as SNR per bit:

$$Eb/N0 = SNR \cdot \frac{BW_{CH}}{Rb} \tag{3-2}$$

where BW_{CH} is the signal of interest bandwidth and the *Rb* is the data rate.

The relation between the BER and Eb/N0 depends on the required communication distance and data rate, the applied modulation scheme, redundancy and demodulation algorithms and implementation. The receiver sensitivity is the lowest power level of the signal of interest at the receiver input, for which the receiver is able to demodulate the information with respect to the required BER. From the modulation scheme and spreading functions of the IEEE802.15.4 (Table 3-1) and BT-LE (Table 3-2), we are able to derive the theoretical relations between BER and Eb/N0 or SNR [101]. In [51] the BERxSNR relations for IEEE802.15.4 (Figure 3-3) and the BERxEb/N0 for BT-LE (Figure 3-4) standards are defined considering the non-coherent demodulation case ([101]) :

IEEE802.15.4

$$BER = \frac{8}{15} \times \frac{1}{16} \times \sum_{k=2}^{16} -1^{k} \binom{16}{k} e^{\left(20 \times SNR \times \left(\frac{1}{k}-1\right)\right)} \tag{3-3}$$

$$BER = e^{-\left(a^2+b^2\right)/2} \left(\sum_{k=0}^{x} \left(\frac{a}{b}\right)^{k} I_k(ab) - \frac{1}{2} I_0(ab) \right)$$

BT-LE

$$a = \sqrt{\frac{(Eb/N0)}{2}\left(1-\sqrt{1-|\rho|^2}\right)} \tag{3-4}$$

$$b = \sqrt{\frac{(Eb/N0)}{2}\left(1+\sqrt{1-|\rho|^2}\right)}$$

$$\rho = \frac{\sin(2\pi\beta)}{2\pi\beta} \qquad \beta = \text{mod. index (0.45 … 0.55)}$$

The quality of the communication is defined in terms of BER or *Packet Error Ratio* (PER). For IEEE802.15.4, the specification is given in terms of PER. In equation (3-2) the spreading sequence is considered in order to define the BERxSNR relation. Knowing the number of bits per packet, we directly derive the BER. Table 3-3 summarizes the requirements for the proposed standards.

We observe that although both standards present similar Eb/N0 requirements, they are related to different BER specifications. The spectrum spreading of the IEEE802.15.4 shows the performance gain when the SNR requirement is relaxed compared to BT-LE. The information from Table 3-3 is the starting point for the system design method of the next section. The derived values of Table 3-3 consider ideal non-coherent demodulation. Since ideal demodulation is inferred, the reference required SNR will be considered with implementation margins.

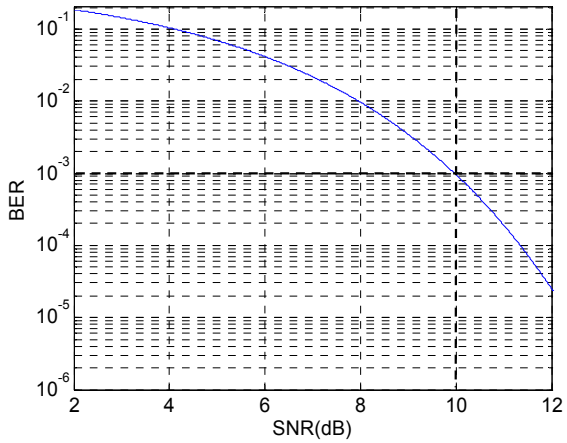


Figure 3-3 : BER x SNR for BT-LE

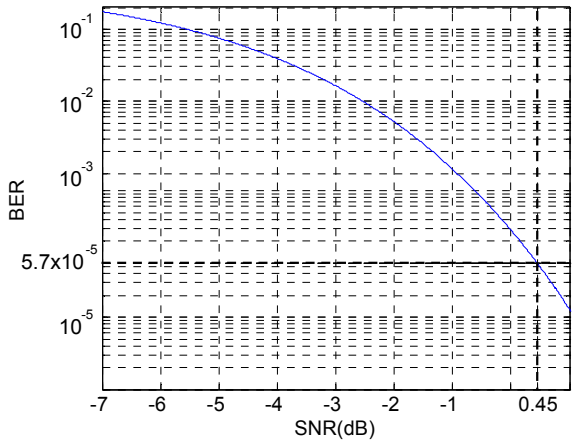


Figure 3-4 : BER x SNR for IEEE802.15.4

Blocker Frequency	IEEE802.15.4	BT-LE
Sensitivity level	-85 dBm	-70 dBm
PER	1%	-
BER	≈5.7×10^{-5}	10^{-3}
Eb/N0	10.35 dB	11 dB
Ec/N0	1.33 dB	-
SNR	0.45 dB	10 dB

Table 3-3 : Sensitivity and BER specifications

2.3 Linearity

In addition to the amplification of the input signal, a receiver also generates a sequence of harmonics. This is the consequence of the non-linear transfer function, which is modeled by a polynomial of order "m":

$$y = \sum_{k=1}^{m} \alpha_k x^k \tag{3-5}$$

The most constraining effect regarding non-linearity happens when a harmonic created by the intermodulation product between two interferers falls into the band of interest (Figure 3-5). The intermodulation case defines the *Input Referred Third Order Intercept Point* (IIP3) test bench. From Figure 3-5, IM_3 falls at $f_0=2\cdot f_{int1}-f_{int2}$, where is located the signal of interest. The IIP3 is defined as the level at the block input which IM_3 is equal to the input Int_n multiplied by the linear gain α_1. Another consequence is the gain saturation/blocking by a strong out-of-band signal, called blocker.

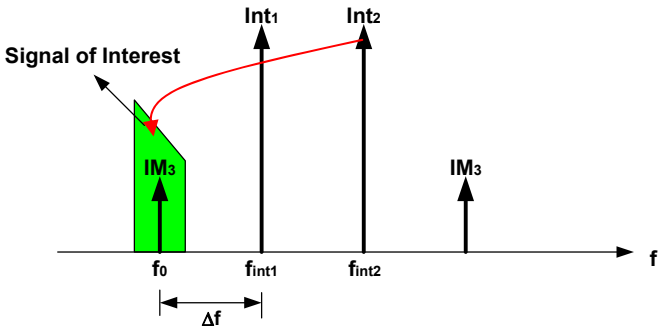


Figure 3-5 : The Intermodulation Problem and the IIP3 Test Bench

At the system level, the IM_3 product is summed to the thermal noise, degrading the SNDR. This impact is manageable by controlling the level of interferer or the level of non-linearity of the block IIP3. The standards specify the level of the interferers at the receiver input and the frequency spacing between the interferer and the closest interferer Δf that needs to be considered. The IEEE802.15.4 standard does not specify IIP3 test bench, but it can be inferred from the interferer profile which are Δf=5MHz and 10MHz away from the signal of interest [102]. Table 3-4 summarizes the interferer levels and spacing from the signal of interest for the IEEE802.15.4 and BT-LE standards:

Parameter	IEEE802.15.4	BT-LE
$Pint_n$	-52 dBm	-50 dBm
Signal of Interest Level	-82 dBm (S+x)	-64 dBm (S+x)
Δf	5 MHz	3, 4, 5 MHz

Table 3-4 : Interferers profile for the IIP3 test bench.

2.4 Channel Selection and the Interference / Blocking Performance

The ability to correctly demodulate a signal in the presence of in-band interferer at a given distance from the signal of interest depends on the channel selection, the in-band rejection and the image rejection. The in-band interference considers a channel of the same standard inside the RF band BW_{RF}. The out-of-band blocking performance of a receiver is the ability to correctly demodulate a signal of interest, in the presence of a strong out-of-band blocker, defined as a continuous waveform tone.

The blockers are strong signals which can saturate a given block in the receiver. From a given non-linear transfer function point of view, we observe that the gain for the signal of interest is attenuated or completely blocked by the receiver saturation. The out-of-band blockers are normally rejected by the RF front-end filter.

An in-band interferer can impact the receiver SNDR in three different ways:

- Spectrum folding level - This phenomenon occurs in mixer (image folding) and sampling (aliasing) operations. Depending on the frequency plan, an in-band interferer which is spaced Δf from the signal of interest might fall into the band of interest, through spectral

folding. The interferer aliasing (sampling process) and the image aliasing (mixing process) are presented in CHAPTER 2.

- ADC resolution - The ADC is typically specified in terms of SNR_{ADC}, which is the ratio between the ADC full scale and the generated quantization noise (dependent on the resolution, i.e. the number of bits). In the case where the full scale is not represented by the signal of interest, but by an interferer, the ADC is scaled by the interference taking into account the difference between the interference and the signal of interest levels in order to respect the required SNR (Figure 3-6).

- Reciprocal mixing and Phase noise intermodulation product - In mixing or sampling process, the signal from the Local Oscillator is actually not a pure harmonic signal. Noise sources add jitter on the phase of the LO from its ideal value, therefore, leading to phase noise. The PSD of the LO down-convert neighbor interferers (adjacent/alternate channel) into the band of interest (Figure 3-7).

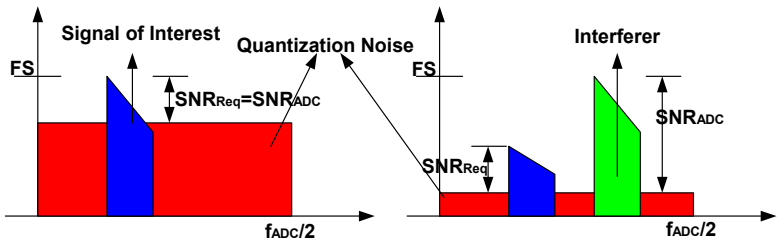


Figure 3-6 : The ADC resolution is presence of an interferer

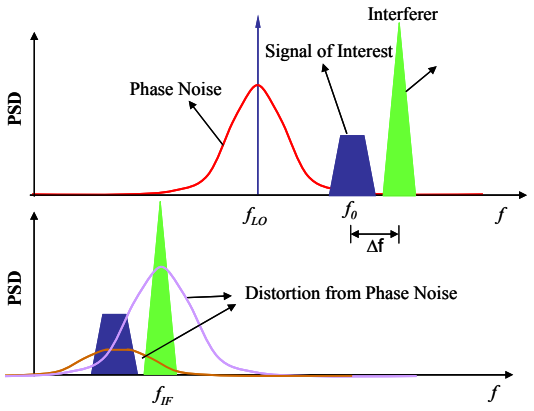


Figure 3-7 : The mixing operation in the presence of phase noise

The standards specify the maximum level of interferers at a given distance Δf for which the receiver must correctly demodulate. These specifications lead to define the frequency plan, filtering techniques and phase noise specifications. Table 3-5 summarizes the out-of-band blocker profile for the proposed standards. Although the IEEE802.15.4 does not specify out-of-band blockers levels, the strongest in-band interferer is taken into account as reference. Table 3-6 summarizes the in-band interferers profile for the proposed standards. For a multi standard receiver design, the phase noise specifications and the interferers' rejection are more constraining in the BT-LE standard if compared to IEEE802.15.4.

Blocker Frequency	802.15.4	BT-LE
30 MHz ~ 2 GHz	-52	-30
2 GHz ~2.393 GHz	-52	-35
2.393 GHz ~ 2.398 GHz	-82	-35
2.498 GHz ~3 GHz	-52	-35
3 GHz ~12.75 GHz	-52	- 30

Table 3-5 : Out-of-band blockers profile (dBm).

Δf	802.15.4	BT-LE
In-band	-88.5	-88
1 MHz	-	-83
2 MHz	-	-50
3 MHz	-	-40
5 MHz	-82	-40
10 MHz	-52	-40
Image	-	-58
Image±1 MHz	-	-52

Table 3-6 : In-band interferers profile (dBm).

Figure 3-8 and Figure 3-9 illustrate the interferer profiles for the proposed standards:

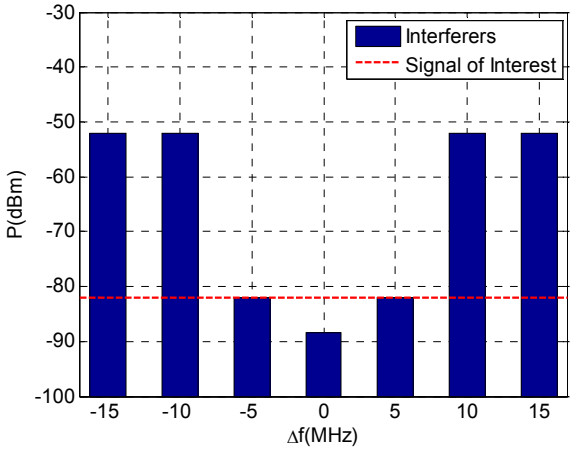


Figure 3-8 : Interferers profile for 802.15.4

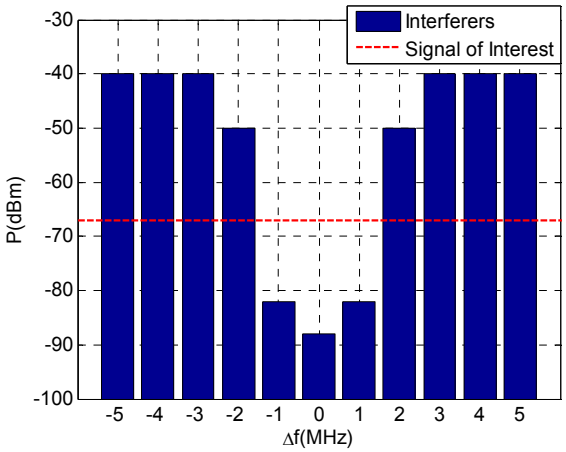


Figure 3-9 : Interferers profile for BT-LE

2.5 Dynamic Range

The IIP3 specification test bench presented in section 2.3 considers the maximum gain configuration. Another test bench which tests non linearity, is the maximum input level, where the signal saturation is taken into account, in this cases IP1 and IIP3 specifications are set. The impact on the receiver facing a strong signal of interest is the same than with blocker or amplifier saturation, therefore, the receiver linearity has also to be evaluated for the maximum input configuration.

In order to set the maximum input level, the minimum distance range between the two transceivers at the maximum allowed transmitted power is considered. The dynamic range is therefore the ratio between the maximum input signal of interest and the sensitivity level. The minimum gain is set between the ADC full scale and the maximum input signal, where the maximum gain is the ratio between the ADC full scale and the filtered strongest close-in interferer (2.4).

	IEEE802.15.4	BT-LE
Sensitivity	-85 dBm	-70 dBm
Maximum input signal	-20 dBm	-10 dBm
Dynamic Range	65 dB	60 dB

Table 3-7 : The proposed standards dynamic range

3 System Level Design Methodology

In this section we present a block specification method where the wideband noise aliasing can be considered between blocks. The basic concept of the method is to separate the blocks constraints in terms of SNR and SNDR degradations per block and then to calculate the system level blocks parameters (G, NF, IIP3). The total SNR and SNDR degradations should respect the minimum allowed SNR defined in Table 3-3 plus an implementation margin at the ADC output. It can be used to study different SNR/SNDR degradation distributions while optimizing the design for a given criterion (ex. power consumption, integration). Once the parameters are calculated, the results are applied on the system level simulation tool in order to evaluate and validate a given architecture and configuration with regards to a given standard. If compared with the method presented in [98], we propose two main improvements: suitability for BPS receivers and ability to apply arbitrary SNR degradation distribution. The methodology is illustrated on the block diagram of Figure 3-10:

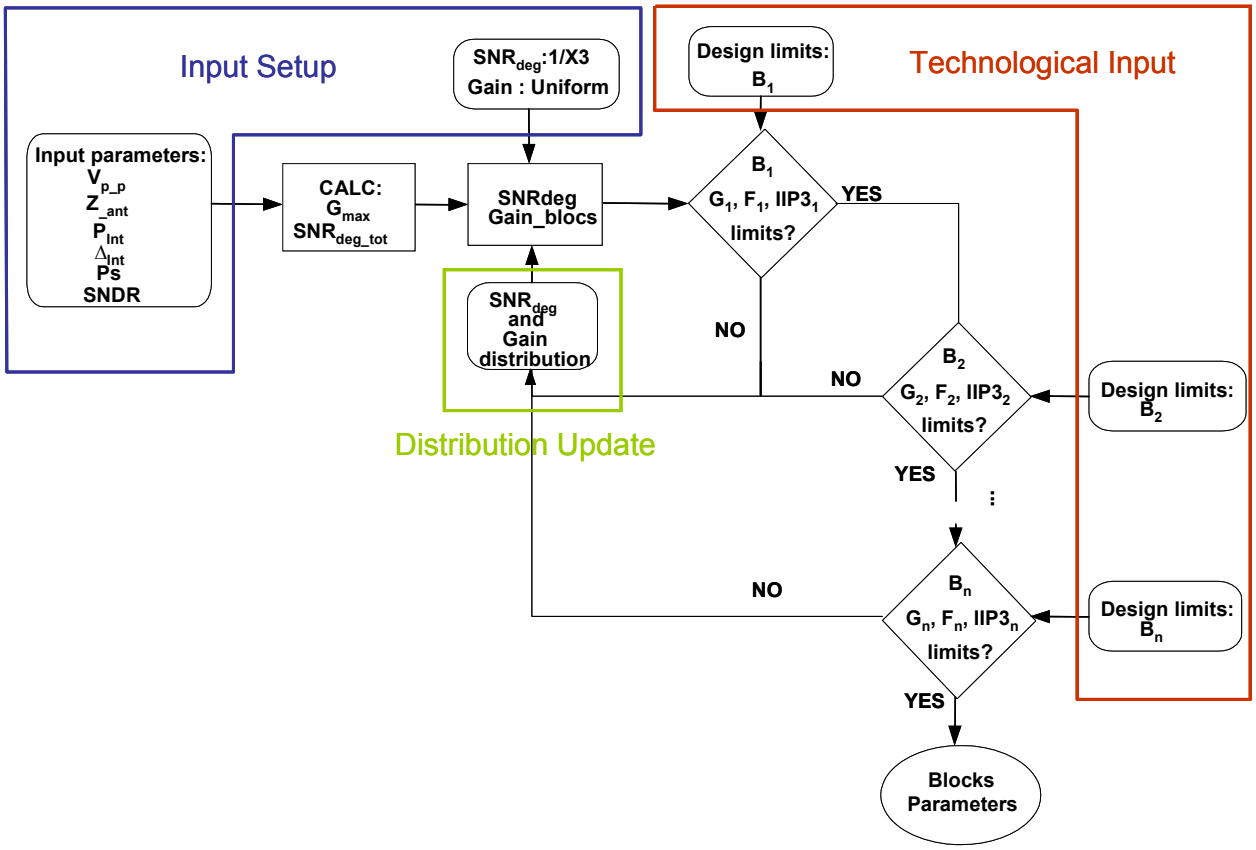


Figure 3-10 : The system level design method algorithm

A set of input parameters for the receiver are defined. The receiver total gain and the allowed SNR degradation are defined depending on the full scale and the strongest signal input at high gain mode. We define a first distribution of gain and SNR/SNDR degradations and the blocks parameters are calculated. The block performance is compared with the state of the art, and whenever these parameters do not fit an actual implementation, the SNR/SNDR and gain distributions are updated. This represents an iterative process which links bottom-up issues from implementation and top-down approach for the standard. On the following we detail the method.

3.1 Definition of ADC Saturation - Maximum Gain and Adjacent Signal Filtering

The first parameter to be analyzed is the receiver maximum gain and the gain distribution. Voltage square calculations are preferred rather than watts. The objective is to define gain and noise figure specifications without considering blocks input-output impedances, letting a degree of freedom for the designer. The signal power at the input is transformed into voltage taking into account the antenna impedance:

$$V_{in}^{\ 2} = P_{in} \cdot \left| Z_{ant} \right| \tag{3-6}$$

From this point, the block gain is the loaded voltage gain, which intrinsically takes into account the blocks input and output impedances. The second point to define the total gain is the maximum voltage swing V_{p_p} at the end of the chain, i.e. the ADC full-scale range.

$$V_{\max}^{\ 2} = \frac{V_{p\_p}^{\ 2}}{8} \tag{3-7}$$

Therefore the maxim allowed voltage gain is:

$$Gv_{\max} = \frac{V_{\max}}{V_{in}} \Delta adj \tag{3-8}$$

The maximum gain is a test bench defined for the minimum signal of interest power at the input. The strongest input signal in the maximum gain mode is at 3MHz distance for BT-LE and 10MHz distance for IEEE802.15.4. From (3-8) we observe that if better interferer rejection Δadj is implemented, more gain can be applied. In consequence, the ADC dynamic range specifications can be relaxed.

A numerical example is calculated for BT-LE standards. Consider the implementation in 65nm CMOS technology, where V_{p_p}=1V is used, the maximum input level on the ADC in V^2 is $V_{max}^{\ 2}$ =1/8. The strongest interferer at the input is P_{int}=-40dBm. Whenever Z_{ant}=50Ω, the maximum input voltage at the maximum gain test is $V_{in}^{\ 2}$=5μV^2. In the worst case, where Δadj_{dB}=0dB, the maximum allowed voltage gain in dB is from (3-8) Gv_{max}(dB)=44dB. The method considers M active blocks on the receiver chain. The gain distribution is set considering implementation constraints and the fact that if most of the gain is implemented at low frequencies, the receiver would consume less power. Nevertheless high gain in early stages in the chain enables to reduce the overall NF. Since the method presents an iterative process, the blocks

gains are updated to a level where blocks gains and NFs are in accordance with the state of the art for low power base blocks.

3.2 Definition of required SNR and SNR degradation (Noise Figure and Noise Aliasing)

After defining the maximum allowed gain, the next step is to define the total allowed SNR degradation. For classical architectures, the total allowed SNR degradation is the same as for the equivalent NF, which is not the case in BPS architecture where noise aliasing occurs. First we define the SNR degradation being the ratio between the block input and output SNR.

$$SNR_{\deg\_i} = \frac{SNR_{in\_i}}{SNR_{out\_i}} \tag{3-9}$$

The total allowed SNR degradation is the ratio between the sensitivity over noise floor (input SNR) and the allowed SNR (output SNR, Table 3-3), defined as follows:

$$SNR_{\deg\_tot} = \frac{P_S}{SNR_{req} \cdot Mar \cdot K \cdot T \cdot BW_{CH}} \tag{3-10}$$

where: P_S=the sensitivity level in Watts, SNR_{req}=the required SNR at the ADC output. Mar=implementation margin for the required SNR, K=Boltzmann constant, T=temperature in Kelvin and BW_{CH}=channel bandwidth that the signal of interest occupies.

As it was defined for the gain, the maximum allowed SNR degradation is split between the M active receiver blocks, where the distribution is dependent on implementation constraints:

$$SNR_{\deg\_tot} = \prod_{i=1}^{M} SNR_{\deg\_i} \tag{3-11}$$

The equivalent NF calculated from Friis formula is equivalent to the parameter SNR_{deg_tot} since it is the ratio between the receiver input and output SNR. The generalization over the SNR degradation makes it possible to add noise aliasing and different distortion sources on the model. Figure 3-11 illustrates the evolution of the noise over the receiver. The total noise at the output of the i^{th} block is the sum in V^2 of the input noise and the input referred generated noise Pn_{bi-1}. The input noise in its turn is the output noise from the previous block Pn_{i-1} multiplied by an aliasing factor γ_I. The blocks NF, F_i, is calculated from the derived Pn_{bi-1}. The different noise sources are multiplied by the square of the block voltage gain (3-12).

$$\left(Pn_{i-1} \cdot \gamma_i + Pn_{bi}\right) \cdot \left(Gv_i\right)^2 = Pn_i \tag{3-12}$$

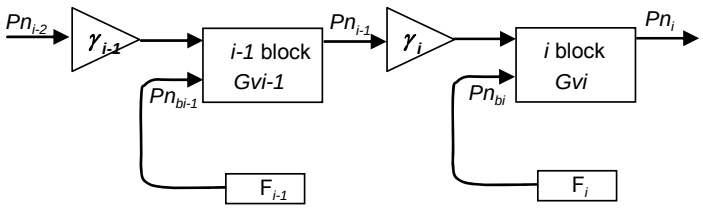


Figure 3-11 : System noise path block diagram

We remind the aliasing factor defined in CHAPTER 2 in the case of a BPS test bench:

$$\gamma = 1 + \frac{2 \cdot BW_{noise} \cdot \Delta n}{fs} \tag{3-13}$$

where: BW_{noise}=equivalent noise bandwidth dependent on the chain cut-off frequency, Δn=band to out-of-band noise ratio, dependent on the anti-aliasing filter and to the pre-sampler gain, fs= sampling frequency. Pn_i is calculated through the gain and SNR_{deg} distributions and the required SNR:

$$Pn_i = \frac{P_s \cdot G_{\max}{}^2}{\prod_{n=i+1}^{M} SNR_{\deg n} \cdot \prod_{n=i+1}^{M} (Gv_n)^2 \cdot SNR_{req} \cdot Mar} \tag{3-14}$$

Finally, since SNR_{degi} and Pn_i are known, we define the possible aliasing factors in the receiver in order to calculate the input referred generated noise (in V^2):

$$Pn_{b\,i} = Pn_{i-1} \cdot \left(SNR_{\deg i} - \gamma_i\right) \tag{3-15}$$

From Pn_i, we define an equivalent F_i referred to Z_{ant}:

$$F_{i\_Zant} = \frac{Pn_{bi}}{K \cdot T \cdot |Z_{ant}| \cdot BW_{CH}} + 1 \tag{3-16}$$

There are other distortion sources that can be added on the block diagram of Figure 3-11, (illustrated in Figure 3-12) and (3-15) is adapted in order to consider these different distortion sources (3-17).

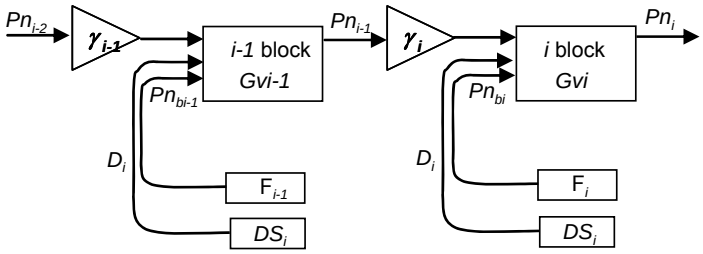


Figure 3-12 : System noise path block diagram with arbitrary additional source of distortion

$$Pn_{b\,i} + D_i = Pn_{i-1} \cdot \left(SNR_{\deg i} - \gamma_i\right) \tag{3-17}$$

This way, the distortion due to phase noise on the mixer and on the sampling operation can be considered on the system level design. The impact of arbitrary jitter on the sampled SNDR and the jitter distortion is presented in CHAPTER 6. On the following section we consider the presence of interferers and also the intermodulation product through the IIP3 test bench. In this case we define an SNDR degradation distribution in order to define the various blocks IIP3.

3.3 Definition of SNDR degradation - IIP3 test bench and specification

Once the Pn_{bi} have been calculated for each block, we proceed to the non-linearity analysis. In the IIP3 test bench, the signal of interest power is defined L_{dB} over the sensitivity level. This means that the initial SNR is L_{dB} over the one defined in the sensitivity test bench. This additional margin SNR is degraded by intermodulation products which defines an SNDR,

therefore a new degradation distribution is set, the signal-to-noise-plus-non-linear distortion ratio SNDR degradation:

$$SNDR_{\deg\_tot} = SNR_{\deg\_tot} \cdot L = \prod_{i=1}^{M} SNDR_{\deg_i} \tag{3-18}$$

Figure 3-13 shows the noise and distortion evolution per block. Regarding the distortion, a source Pd_{bi} is defined referred to the output. For a required SNDR, the block noise–plus-distortion level Pnd_i is defined to derive the non-linear distortion level Pd_{bi} per block. The Pnd_i is defined as follows:

$$Pnd_i = \left(Pn_{bi} + Pnd_{i-1} \cdot \gamma_1\right) \cdot \left(Gv_i\right)^2 + Pd_{bi} \tag{3-19}$$

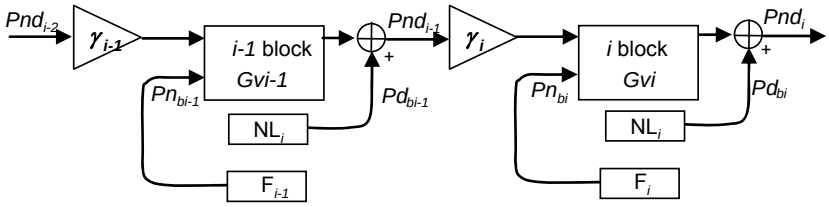


Figure 3-13 : System noise plus distortion path block diagram

The allowed distortion generated by the block referred to the output Pd_{bi}, is defined as follows:

$$Pd_{bi} = \left(Gv_i\right)^2 \cdot \left(Pnd_{i-1} \cdot \left(SNDR_{\deg i} - \gamma_i\right) - Pn_{bi}\right) \tag{3-20}$$

Once Pd_{bi} are defined we can estimate IIP3 specifications. Consider a third order polynomial:

$$v_{out} = Gv_i \cdot v_i + \alpha_3 \cdot v_i^{\,3} \tag{3-21}$$

Now consider two interferers Int_1 and Int_2 at the input of a block implementing the transfer function of (3-21) and an intermodulation product IM_3 (Figure 3-5) which in this case is defined to be equal to allowed generated distortion referred to the output Pd_{bi} since the intermodulation falls in the band of interest. The intermodulation product is given by:

$$Pd_{bi} = \left(\left(\frac{3}{4} \cdot \alpha_{3i} \cdot Int_{1i}^{\,2} \cdot Int_{2i}\right) \Big/ \sqrt{2}\right)^2 \tag{3-22}$$

The input referred third order intercept point is the input when the linear gain is equal to the third order intermodulation product:

$$IIP3_i\left(V^2\right) = \left(\frac{4}{6}\left|\frac{Gv_i}{\alpha_{3i}}\right|\right) \tag{3-23}$$

Applying (3-22) into (3-23), and defining the IIP3 in dBmW referred to the antenna impedance we obtain:

$$IIP3_i\left(dBmW\right) = 10 \cdot \log 10\left(\frac{\sqrt{2}}{2}\left|Gv_i \cdot \frac{Int_{1i}^{\,2} \cdot Int_{2i}}{\sqrt{Pd_{bi}}}\right|\right) + 30 - 10 \cdot \log 10\left(\left|Z_{ant}\right|\right) \tag{3-24}$$

Int_{1i} and Int_{2i} from (3-24) are defined in Table 3-4. In a worst case, where there is no interferer rejection, Int_{1i} and Int_{2i} undergo the same gain of the signal of interest. Whenever the interferers can be rejected by Δint_{1i} and Δint_{2i}, the interferers' amplitudes are defined as follows:

$$Int_{1i} = Int_{1\_0} \cdot \prod_{n=1}^{i} \left(Gv_i \cdot \Delta \text{int}_{1i}\right)^2 \tag{3-25}$$

$$Int_{2i} = Int_{2\_0} \cdot \prod_{n=1}^{i} \left(Gv_i \cdot \Delta \text{int}_{2i}\right)^2 \tag{3-26}$$

IIP3 specifications can be strongly relaxed in receivers if an interferer rejection process is implemented. For blocks where the linearity is critical in terms of power consumption, the value for $SNDR_{deg}$ can be increased for that matter.

3.4 Definition of the Filtering Specifications - Anti-aliasing, Image and Aliasing Interferer Rejection

Three filtering characteristics are already introduced on the method, the adjacent rejection Δadj, the anti-aliasing filtering Δn and the interferers' rejection on the IIP3 test bench, Δint_1 and Δint_2. Although these specifications strongly rely on the receiver performances, there is no fixed filtering mask for them for the analog part. In other words, the receiver could correctly demodulate the signal, respecting the standard, by applying the digital base band filter only, for signals which are not aliased into the band of interest: adjacent, IIP3 interferers.

In this section we present test cases where the filtering function can not be avoided and a level of rejection is explicitly defined, therefore a filtering mask can be derived. There are two major aspects to consider the filtering specifications: the image rejection and the aliasing interferer rejection, which is particular to BPS architectures. The image and the aliasing interferer problems are presented in CHAPTER 2 where we observe an in-band channel being aliased into the band of interest after a mixing or a sampling process due to the distance between the signal of interest and the interferer.

As it was defined for the IIP3 test bench, the signal of interest power is defined L_{dB} over the sensitivity level in the presence of interferers. In this case, the interferer can be either one of the aliasing interferers from the BPS process or the image signal. The interferer is filtered prior to aliasing and the residual power falls in the band of interest degrading the SNDR. The interferers' test benches are considered one by one, which means that only one aliasing occurs per test bench. The margin L is the ratio between the sum of the distortions (noise and aliased interferer) and the initial noise floor power, which is the noise floor PSD integrated in BW_{CH}:

$$L = \frac{Pn_{floor} + D_{alias}}{Pn_{floor}} \tag{3-27}$$

$$Pn_{floor} = \frac{P_S}{SNR_{req} \cdot Mar} \tag{3-28}$$

From the defined margin and the interferers profile we can infer the required rejection (in linear gain) which gives the maximum allowed aliasing distortion:

$$\Delta \text{int}^2 = \frac{P\,\text{int}}{\left(L - Pn_{floor}\right)} \tag{3-29}$$

where Pint is the interferer power (V^2) for the given test bench (image or aliasing interferer). Another important point to define is that as long as the aliasing do not occur, the required Δint can be divided into different filtering techniques. Consider the ULP standards presented in section 2. The sensitivity level and the required SNR are presented in Table 3-3. The implementation margin is considered $Mar_{dB\_IEEE802.15.4}$=3dB and $Mar_{dB\_BT\text{-}LE}$=4dB. The interferer profiles are presented in Figure 3-8 for IEEE802.15.4 and Figure 3-9 for BT-LE. For both standards the margin L_{dB} is L_{dB}=3dB. The image signal level for BT-LE is presented in Table 3-6. With the information section 2 and (3-29) we derive the aliasing and image interferers' rejection:

	IEEE802.15.4	**BT-LE**
Image rejection	-	26 dB
Aliasing interferer rejection	36.5 dB	44 dB

Table 3-8 : Aliasing and image signal rejection

3.5 ADC equivalent NF and IIP3 into resolution and SFDR

From section 3.2 and given SNR degradation and gains distributions, we define the NF for each active block. From the SNDR degradation, the IIP3 per block is defined. In this section we translate the equivalent NF and IIP3 defined for the last block, the ADC, into specifications which the ADC designers are more used to: the effective number of bits and the *Spurious Free Dynamic Range* (SFDR).

3.5.1 Flat Quantization Noise ADC

The NF of an ADC has contributions from thermal noise and quantization noise. The definition of "effective number of bits", considers all the noise sources into one, the quantization noise. In practice, the noise coming from thermal sources for high-resolution ADCs can be even higher than the quantization noise, where there is more than one bit difference between the implemented number of bits and the effective number of bits. The quantization PSD (V^2/Hz) generated by the ADC is proportional to the effective number of bits n_{beff}, the full-scale voltage swing V_{p_p}, and the ADC sampling frequency f_{ADC} [97]. For quantization noise where the distribution is uniform (the noise PSD is flat over the frequency), the PSD is defined as follows:

$$PSD_{ADC} = \left(\frac{1}{12}\left(\frac{V_{p\_p}}{2^{n_{eff}}}\right)^2 \frac{2}{f_{ADC}}\right) \left(V^2/Hz\right) \tag{3-30}$$

Applying (3-10) on (3-16), we derive relation between the equivalent noise figure referred to the antenna impedance and the ADC effective number of bits:

$$n_{beff} = \left\lceil \log 2\left(\sqrt{\frac{2}{f_{ADC}} \cdot \frac{1}{12} \cdot \frac{V_{p\_p}{}^2}{K \cdot T \cdot |Z_{ant}|} \cdot \frac{1}{\left(F_{ADC} - 1\right)}}\right)\right\rceil \tag{3-31}$$

where $\lceil\ \rceil$ represents the ceiling function.

3.5.2 ΣΔ - ADCs

We observed from (3-31) that the equivalent ADC noise figure can be decreased if f_{ADC} increases even for constant resolution. This happens since the noise in DT system is considered inside the band $-f_{ADC}/2$ to $f_{ADC}/2$; although the total noise does not change, the increasing of the sampling frequency decreases the equivalent PSD. This behavior increases ADC SNR by over sampling. A special type of converter which is particularly adapted to over sampling is the ∑Δ ADC [103], because the quantization noise is modulated and not flat over the Nyquist-Shannon range. The equivalent noise PSD for ∑Δ of order L, sampling frequency f_{ADC} and resolution n_{beff} is given by [103]:

$$PSD_{ADC\_\Sigma\Delta}(V^2/Hz) = \left(\frac{1}{12}\left(\frac{V_{p\_p}}{2^{n_{eff}}}\right)^2 \frac{2}{f_{ADC}}\right) \cdot 4\left[\sin\left(\frac{\pi f}{f_{ADC}}\right)\right]^{2L} \tag{3-32}$$

We observe that the PSD is concentrated at higher frequencies, since the ∑Δ noise transfer function behaves as a high-pass filter. The equation which links the equivalent NF to the effective number of bits becomes:

$$n_{beff} = \left\lceil \log 2\left(\sqrt{\left(\frac{2}{f_{ADC}}\right)^{2L+1} \cdot \frac{(BW_{CH})^{2L}}{12} \cdot \frac{(2L+1)}{\pi^{2L}} \cdot \frac{V_{p\_p}{}^2}{K \cdot T \cdot |Z_{ant}|} \cdot \frac{1}{(F_{ADC}-1)}}\right) \right\rceil \tag{3-33}$$

where ⌈ ⌉ represents the ceiling function.

We observe that for L=0 we obtain the same function than for a flat quantization noise ADC and that increasing of the ∑Δ order decreases the quantization noise inside the band of interest for the same number of bits and over sampling ratio $2 \cdot BW_{CH}/f_{ADC}$. In conclusion, the gain in SNR with over sampling becomes more interesting as the order to the ∑Δ increases, but we must consider that stability and technological issues arise as drawbacks by limiting the potential order.

3.5.3 SFDR and IIP3

In an ADC validation test bench, the SFDR is the ratio between the fundamental signal on the ADC input (full scale range) and the strongest spurious signal at the input, given in dBFS (dB full scale). Considering that the strongest spurious is a result of third order coefficient of the polynomial of (3-21) we can define the third order coefficient α_3 in terms of SFDR [104] (3-34). The input referred third order intercept point is the input when the linear gain is equal to the third order intermodulation product, where the IIP3 is linked with α_3 by (3-23). Applying (3-23) into (3-22), and defining the IIP3 in V_{RMS}, we obtain (3-35).

$$SFDR = \left(\frac{1}{\left(\frac{V_{p\_p}}{2}\right)^2 \cdot \alpha_3} + 1\right)^2 \tag{3-34}$$

$$SFDR = \left(\frac{8}{V_{p\_p}^{\ 2}} \cdot IIP3 + 1 \right)^2 \tag{3-35}$$

4 System Level Simulation Tool

Since the wideband spectrum aliasing is to be verified for the BPS process, it is impractical to apply complex envelope modeling. Different frequency components may fall in the band of interest after BPS, for example an intermodulation product from an interferer and the signal of interest itself. For IIP3 specifications, these different test benches particular to BPS have also to be verified. The proposed tool present a frequency domain analysis approach, where the parameter to validate the receiver chain is the SNDR x Block calculated inside the band occupied by the signal of interest.

4.1 Basic Simulation Flow

Vector processing is applied on the tool to generate different time truncated signals (signal of interest, noise, interferer, non linear distortion) which are processed block per block. The basic simulation flow is illustrated in Figure 3-14:

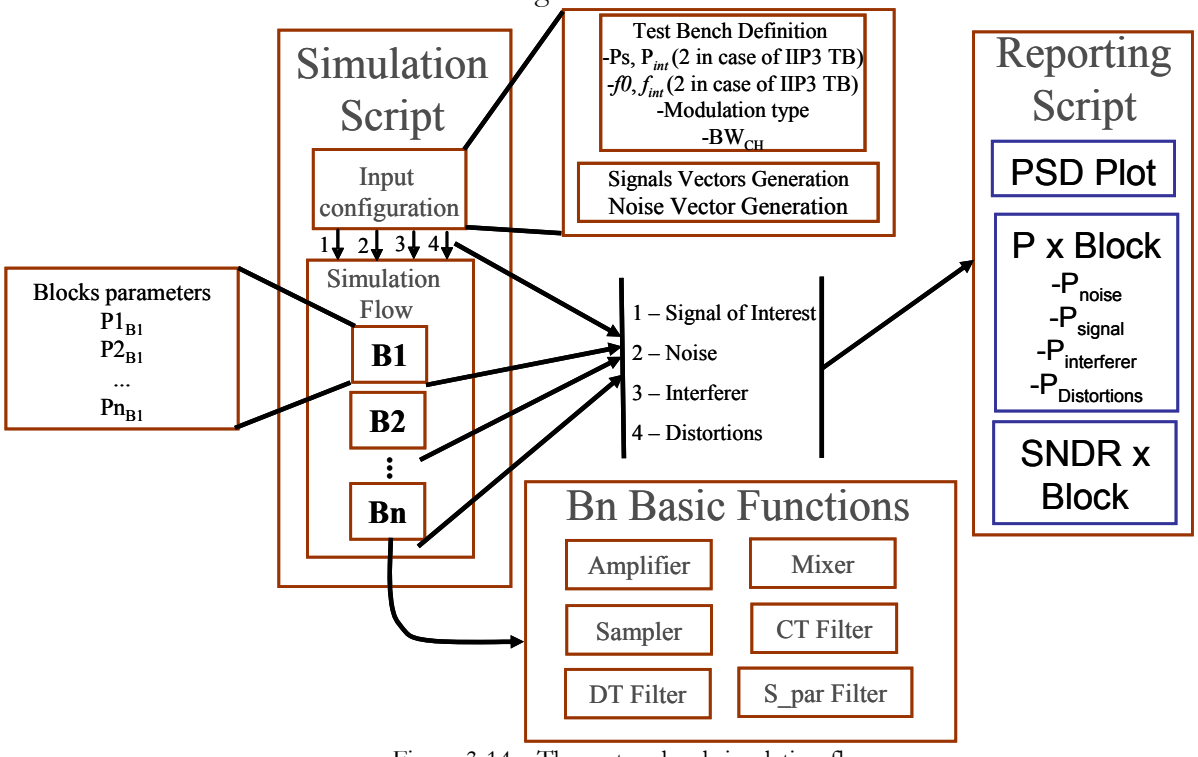


Figure 3-14 : The system level simulation flow

There are two main files, the simulation and the reporting scripts. On the simulation script there are two main parts: the input configuration and the receiver blocks flow. In the input configuration the test bench is defined and a structure signal is generated. The structure signal contains four different natures of signals: the signal of interest, the interferer, the noise and distortions. These different signals are processed separately inside the basic blocks. The nodes of

the architecture are then defined putting in order the functional blocks depending of the architecture type (homodyne, heterodyne, BPS, etc…); at the output of each block, the structure signal is saved into a file labeled by a node.

The basic block is modeled by different fundamental functions, which are detailed on the following sub-sections. After the simulation is finished, it is possible to visualize the blocks output PSD, for each type of signal separately. Inside the band occupied by the signal of interest, we calculate the power for each type of signal. Hence, the simulator is able to discriminate the different contributions to SNDR degradation enabling parameter optimizations. The different signals power and the resulting SNDR is analyzed per block. On the following sections we detail the block and fundamental function modeling, how different architectures and imperfections can be evaluated.

4.1.1 Generating the Input Configuration and Signals

As observed in Figure 3-14, the input configuration file contains information about the test bench and the different signals are generated inside. The structure test bench is a variable containing the input configuration on the receiver which defines a given test. Figure 3-15 summarizes the structure test bench. The definition of the standard brings information on the modulation type, shaping filter and data rate of the required standard. A library is developed for IEEE802.15.4 and BT-LE standards. BW_{CH} defines in which band we want to evaluate the signal of interest and other signals powers. In the case the base band filter is the same than the modulation shaping filter, the evaluation BW_{CH} is the same than that defined by the standard. The test bench structure also contains information about the signal of interest and the interferer power (P_S, P_{int}) and center frequency (f_0,f_{int}), the input noise PSD (in V^2/Hz), which depends on the simulation temperature and antenna impedance. Considering the noise as an *Ergodic* signal, different number of realizations N can be defined in order to have better noise estimation.

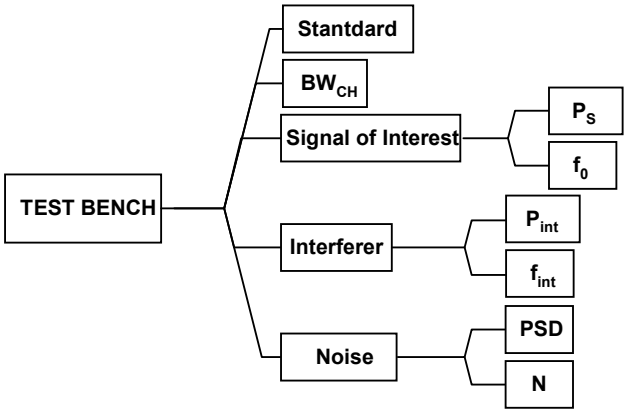


Figure 3-15 - TB structure

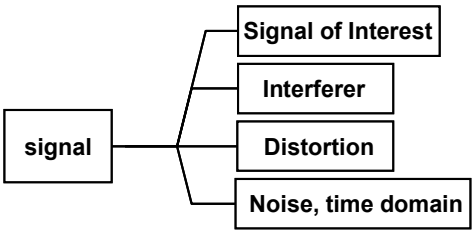


Figure 3-16 - Signal structure

For the Signal of Interest and for the Interferer, as defined in the previous sections, the modulated signals have to be verified in order to check if the first and last points are the same to create a periodic signal from a random signal. This enables having precise estimations on the DSP through FFT analysis. As presented on Figure 3-14, the input signal vectors are generated from the defined test bench. A structure signal integrates the different signal vectors, illustrated in Figure 3-16. The structure signal is the input for the blocks simulation flow. At the output of the block, the structure signal is saved for spectrum evaluation and visualization.

4.2 Mathematical Principles on the System Level Simulation Tool

4.2.1 Time Step, Frequency Step and Synchronous Sampling - The Key to Hybrid Time Domain / Frequency Domain Simulation

Differently from Complex Envelope Base Band simulation, the Wide Band Simulation is an inherent requirement to simulate BPS process. We do so in order to visualize and evaluate all the possible aliasing products in this process, and how different filtering techniques can reduce the impact of such aliasing. From section 2, we show that the proposed application is for the ISM band (2.4GHz to 2.48GHz). The simulated circuit has at least a bandwidth of the highest RF frequency to be addressed. For that the time step (T_{step}) and frequency resolution (f_{step}) are defined. The beginning of the simulation flow consists in defining these two inputs. The time step must be consistent with the front-end cut-off frequency, to correctly simulate the aliasing noise as defined in CHAPTER 2. The simulated architectures of CHAPTER 4 present equivalent noise bandwidths of BW_{noise}=3GHz, defining the time step. The frequency step is linked to how precisely we want to evaluate the power of a signal. By definition, the power spectral density of a random process is [7]:

$$S_x(f) = \lim_{T\to\infty} \frac{E|X_T(f)|^2}{T} \tag{3-36}$$

where: $X_T(f)$ is the truncated Fourier Transform of a random process where the stop time is defined by T. The longer is T the more simulated points Np we have, therefore the frequency step is given by:

$$f_{STEP} = \frac{1}{T_{step}} \cdot \frac{1}{Np} \tag{3-37}$$

In FFT and spectral representation, the process of synchronous sampling [105] can be applied in order to avoid Gibbs phenomenon ([106]) FFT spectral analysis (Figure 3-17). APPENDIX A details the synchronous sampling. To sum-up, the total simulated time has to be an integer multiple of the lowest simulated frequency, i.e. the sampling rate is synchronized with the lowest frequency of the signal to be analyzed. Although a random signal has no periodic characteristics, our test benches are forced to be periodic, by testing if the first and last simulated points are the same.

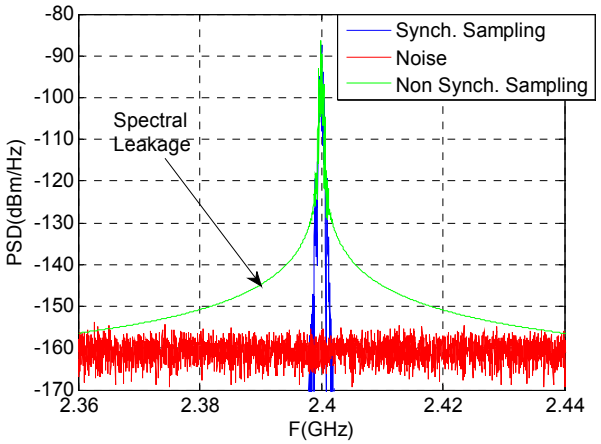


Figure 3-17 -The signal spectra with and without synchronous sampling

4.2.2 The Bussgang Theorem - Signal Non Linearity Decorrelation and Saturation

When a signal undergoes a non-linear transfer function (defined in (3-38)) (for example the signal of interest of the structure signal of Figure 3-16), two distinct parts are observed on the output signal : the first is correlated to the signal and represents saturation (α_3 is negative considering a circuit saturation) and the second is orthogonal to the signal and represents a parasitic signal impacting on the SNDR (3-39):

$$v_{out} = g \cdot v_i + \alpha_3 \cdot v_i^{\,3} \tag{3-38}$$

$$\alpha_3 \cdot v_i^{\,3} = A \cdot v_i + D \tag{3-39}$$

Since in the simulation tool the different signals are analyzed separately, we are interested to calculate $A \cdot v_i$ and D from (3-39). After passing through (3-38) and calculating $A \cdot v_i$ and D (3-39), the parasitic signal D is summed to the Distortion vector of the structure signal (Figure 3-16) and the remaining correlated signal at the block output is derived:

$$v_{COR\_out} = (Gv + A) \cdot v_i \tag{3-40}$$

To calculate the correlation factor A, the proposed system level simulation tool applies the Bussgang theorem [107]. We demonstrate the application of the Bussgang theorem in frequency domain in APPENDIX B , where $A_{[f1,f2]}$ is calculated inside the band f[f1,f2], which is the band occupied by the signal of interest (3-41):

$$A_{[f1,f2]} = \frac{\left\langle v_i, \alpha_3 \cdot v_i^{\,3} \right\rangle_{[f1,f2]}}{\left\| v_i \right\|^2_{[f1,f2]}} \tag{3-41}$$

Figure 3-18 illustrates the output spectra from (3-38) before separation of correlated signal and distortion. Figure 3-19 illustrates the outcomes before and after applying the theorem. Notice that since the non-linear product A is actually sign inverted, it represents the signal saturation. It acts as a compression gain: the ideal gain g is turned into effective gain ($\alpha 1+A$). The remaining distortions are non-correlated to the signal and particular in this case, where only the signal of interest is at the input, it is very low compared to the signal of interest level.

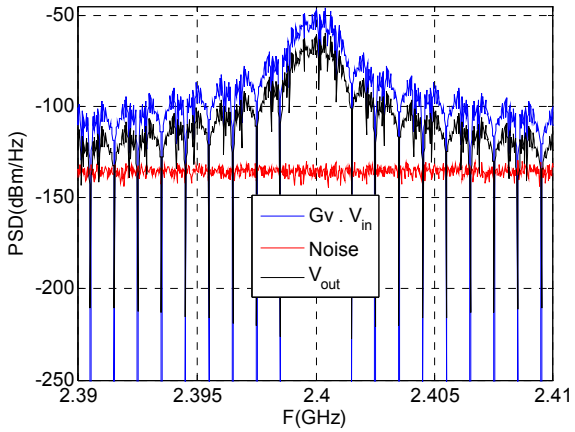


Figure 3-18 - Output Spectra from (3-38)

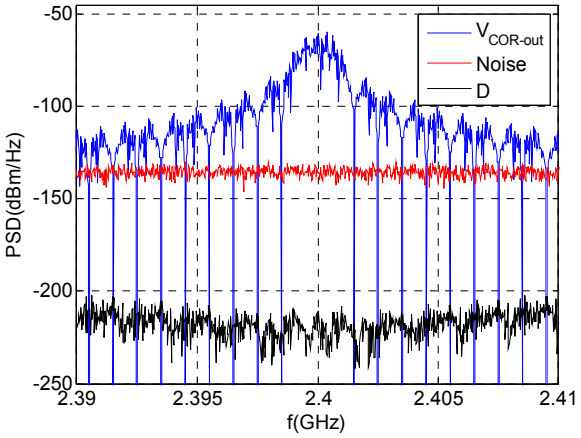


Figure 3-19 - Spectra separation after Bussgang Theorem

The derived SNDR inside the band of interest is therefore the ratio between the PSD of V_{COR_out} integrated between [f1,f2] divided by the PSD of the sum of Noise and D integrated between [f1,f2]:

$$SNDR_{[f1,f2]} = \frac{\left\| v_{COR\_out} \right\|^2_{[f1,f2]}}{\left\| noise + D \right\|^2_{[f1,f2]}} \tag{3-42}$$

The Bussgang theorem may be applied to various applications other than the non-linear polynomial. Another application is on the Phase Noise impact on BPS SNDR, detailed in CHAPTER 6.

4.3 Base Blocks Modeling

4.3.1 Non Linear Noisy Amplifier

In a system level simulation environment, amplification blocks such as LNAs, op-amps, VGAs present three major parameters to be considered: the loaded *Voltage Gain* (Gv), the *Input Referred Third Order Intercept Point* (IIP3), referred to the antenna impedance Z_{ant}, and the *Noise Figure* NF(dB), referred to Z_{ant}. From the basic polynomial defined in (3-38) α_3 is defined as follows [97]:

$$\alpha_3 = -\frac{4}{6}\frac{Gv}{IIP3^2} \tag{3-43}$$

IIP3 is given in V_{RMS}. The total signal at the input v_i actually contains three different signals:

$$v_i = S_{IN} + I_{IN} + D_{IN} \tag{3-44}$$

where S_{IN}, I_{IN} and D_{IN} are the signal of interest, the interferer and non-correlated distortion at the blocks input respectively. Similarly to (3-40), we first calculate the output for the signal of interest:

$$S_{OUT}(f) = S_{IN}(f) \cdot (Gv + A) \tag{3-45}$$

"A" represents the saturation of $S_{IN}(f)$ and is calculated as follows (S_{IN} occupies the band [f1,f2]):

$$A_{[f1,f2]} = \frac{\left\langle S_{IN}, \alpha_3 \cdot V_i^3 \right\rangle_{[f1,f2]}}{\left\| S_{IN} \right\|^2_{[f1,f2]}} \tag{3-46}$$

The same procedure is applied for the interferer. (I_{IN} occupies the band [f3,f4]):

$$I_{OUT}(f) = I_{IN}(f) \cdot (Gv + B) \tag{3-47}$$

$$B_{[f3,f4]} = \frac{\left\langle I_{IN}, \alpha_3 \cdot V_i^3 \right\rangle_{[f3,f4]}}{\left\| I_{IN} \right\|^2_{[f3,f4]}} \tag{3-48}$$

"B" represents the saturation of $I_{IN}(f)$. The distortion *D*, which is added noise due to distortion, and is not correlated neither to the signal of interest nor to the interferer, is calculated as follows::

$$D_{OUT}(f) = D_{IN}(f) \cdot Gv + \left(\alpha_3 \cdot V_i^3(f) - A \cdot S_{IN}(f) - B \cdot I_{IN}(f)\right) \tag{3-49}$$

The application of such technique enables to have more precise IIP3 evaluation than classical approach. In a wideband system, the linear gain is not constant for all the frequencies, whereas a transfer function is more exact for the behavioral modeling. The transfer function is calculated in frequency domain by the multiplication between the frequency response and the input spectra. Detail on the filtering modeling is given on the following section 4.3.2.

An independent random signal generation models the NF of the block. The NF is defined as the ratio in dB between the total system noise and the noise that would be present if the system was noiseless but excited by input noise from a source at temperature T=297°K [97]. The NF is referred to given impedance which is the noise source resistance. The measurement of the NF is given referred to 50Ω when the block to be tested is excited by a 50Ω noisy source. In the simulation tool all NF are referred to the antenna impedance which in this case sets the transfer from power to voltage domain. Therefore, the input referred generated noise PSD (V^2/Hz) is given by:

$$PSD_{ng} = 4 \cdot \psi^2 \cdot K \cdot T \cdot \mathrm{R} \cdot (F-1)\left(V^2/Hz\right) \tag{3-50}$$

$$\psi = \frac{Z_{in}}{Z_s + Z_{in}} \tag{3-51}$$

Consider the case when the blocks are impedance matched, ψ=0.5. In the specification input, we consider that all NF are referred to 50Ω and matched. After calculating the equivalent input referred generated noise PSD (3-50), we defined the process variance σ_{ng}, in order to generate a random variable ng(t) with Gaussian distribution equivalent noise bandwidth BW_{noise}:

$$\sigma_{ng}^{\ 2} = PSD_{ng} \cdot BW_{noise} \tag{3-52}$$

In a simulation environment, the simulation time step defines $BW_{noise}=1/T_{step}$, which is defined prior to the simulation. Since the noise source is a Gaussian independent random process, the noise is an egordic process. In order to have a good estimation of the noise power spectral density, multiple samples of the noise is generated, then the FFT is calculated for the whole and an average value is used. If a block has a noise PSD which is not flat in the frequency domain, and if the spectral shape is different from the blocks frequency response, then the

reference noise PSD is generated and further filtered. Finally the output noise is computed by the sum of each generated noise implementation with each noise input implementation n_M:

$$n_{out}(t)_M = \left(n_g(t)_M + n_{in}(t)_M\right) \cdot Gv \tag{3-53}$$

4.3.2 Continuous Time and Discrete Time Filters

In the wideband simulation context, the filtering function must be validated for various type of signals: distortions, interferers, and noise. When filtering functions are taken into account in the simulation tool, it is possible to verify if given filter types or orders exhibit the required rejection performance, for example regarding anti-aliasing filter or adjacent channel rejection one for IIP3 specifications.

The filtering operation in the frequency domain gives a much faster result compared to the time domain counterpart calculation. CT and DT filtering functions can be evaluated. The CT filtering function is calculated through Laplace Transform for different filter types: Butterworth, Chebyshev, elliptic and others. Regarding the simulation tool, the input parameters for CT filters consist on the filter type, order, band pass, in-band ripple and zero transmission positions when applicable. For DT filtering, the filter frequency response is computed through the *Fast Fourier Transform* (FFT) algorithm, where the filter coefficients are directly defined by the user. In order to include measurement results in the simulation chain, especially regarding RF front-end filters where S2P parameter files are available, the Touchstone file is read by the simulation tool and the frequency response is applied directly on the various signals.

4.3.3 Non-Linear Noisy Mixer

The main motivation for frequency domain calculation over filtering functions is to avoid long processing time inherent to convolution operations in the time domain. The mixing operation consists in multiplying two input signals in the time domain, of which one is a periodic signal from the LO. In this case, the structure signal (defined in section 4.1.1) and the mixing signal are defined in the frequency domain. The mixing operation is defined as follows:

$$Y(f) = \Im\left[\Im^{-1}(OL(f)) \cdot \Im^{-1}(X(f))\right] \tag{3-54}$$

$\Im$ stands for Fourier Transform. In a MATLAB environment the *Fourier* and *Inverse Fourier Transform* for discrete signals are implemented by the "FFT" and "IFFT" functions respectively. This change towards time domain and backwards frequency domain avoids convolution operations and leads to a huge amount of total simulation time gain. The mixing signal is defined by its center frequency and phase. N multiple harmonics can be defined by the user with amplitude An =1:

$$OL(f) = \sum_{n=1}^{N} An\left(\delta(f - n \cdot f_{ol}) + \delta(f + n \cdot f_{ol})\right) e^{j\varphi f / fOL} \tag{3-55}$$

At this stage the mixing signal is considered to be a perfect Dirac Pulses stream in the frequency domain, therefore, the system tool does not take into account the impact of phase noise on the signal SNDR. The impact of phase noise and jitter on the mixing and sampling operations is subject of a further in-depth study to be presented in CHAPTER 6.

The mixer is modeled by a first non-linear amplifying stage, which infers that the major part of the non-linear products is obtained before the mixing operation. When observing classical Gilbert Cell mixer [37] the input gain stage is the main source of non-linearity. The first parameters for the non-linear noisy mixer are Gv and IIP3. At the mixing input, the signals $S_{OUT(f)}$, $I_{OUT(f)}$ and $D_{OUT(f)}$ are obtained from (3-45), (3-47) and (3-49), respectively. The mixing operation, which is linear, can be applied for each signal type separately. On the following, the mixing operation is applied:

$$S_{OUT\_M}(f) = \Im\left[\Im^{-1}(OL(f)) \cdot \Im^{-1}(S_{OUT}(f))\right] \tag{3-56}$$

$$I_{OUT\_M}(f) = \Im\left[\Im^{-1}(OL(f)) \cdot \Im^{-1}(I_{OUT}(f))\right] \tag{3-57}$$

$$D_{OUT\_M}(f) = \Im\left[\Im^{-1}(OL(f)) \cdot \Im^{-1}(D_{OUT}(f))\right] \tag{3-58}$$

The mixer noise is also referred to the input. The mixing operation aliases the noise from the image frequency of the signal of interest (figure of section MIXER CHAPTER 2). The generated noise PSD_{ng} is given by:

$$PSD_{ng} = 4 \cdot \psi^2 \cdot K \cdot T \cdot R \cdot \left(F_{SSB}/2 - 1\right)\left(V^2/Hz\right) \tag{3-59}$$

$$n_{out}(t)_M = \left[\left(n_g(t)_M + n_{in}(t)_M\right) \cdot Gv\right] \cdot \Im^{-1}(OL(f)) \tag{3-60}$$

4.3.4 Non-Linear Noisy Sampler

For frequency transposition blocks, the sampler is an extension of the mixer. The sampling process is in the frequency domain a convolution by a sequence of Dirac pulses with a period of fs. Consider a finite sequence in a simulation environment containing N+1 points: the sampling operation is a multiplication by a sequence of Dirac pulses in the time domain:

$$x_S(t) = \sum_{n=0}^{N \cdot \frac{Tres}{Ts}} x_C(t) \cdot \delta(t - nTs) \tag{3-61}$$

In order to implement the sampling process in the time domain, there are two techniques: we either generate the sequence of Dirac pulses in the time domain and multiply with the signal to be sampled, or decimate the time domain signal (defined in T_{res}), considering one point every Ts. For the former, the generation of the Dirac pulses leads to long "for" loops at high sampling frequencies and high N (3-61). For the latter, the sampling frequency Ts needs to be an integer multiple or T_{res}. Considering the coherent sampling, where the frequency step is defined by $f_{step}=1/(N \cdot T_{res})$, any multiple of f_{step} can be correctly represented in the frequency domain without spectral leakage. The sampling process using the time domain decimation should respect both concepts: fs/f_{step} is an integer and f_{res}/fs, limiting to a few different possible sampling frequencies.

We propose to generate the Dirac pulse sequence in the frequency domain then to pass to time domain using IFFT. This technique makes it possible to respect the fs/f_{step} integer condition and avoid long "for" loops.

$$S(f) = \sum_{n=0}^{fres/fs} An\left(\delta(f - n \cdot f_S) + \delta(f + n \cdot f_S)\right) e^{j\varphi f/f_S} \tag{3-62}$$

$$Y(f) = \Im\left[\Im^{-1}(S(f)) \cdot \Im^{-1}(X(f))\right] \tag{3-63}$$

We observe that the number of pulses from (3-61) to (3-62) is strongly reduced considering high sampling frequencies ($fs > 10 \cdot f_{step}$). The gain is applied after the sampling operation. Like in the mixing operation, the non-linear polynomial is applied prior to sampling. As long as f_{res} is high enough to consider the entire front-end bandwidth, the complete phenomenon of noise aliasing is observed. While generating the Dirac sequence in the frequency domain, any integer sampling frequency multiple of f_{step} can be used. Another application is to set as the sampling signal the Fourier Transform of different signal types (delta functions, non uniform sampling, sampling in presence of jitter).

While applying the modeled anti-aliasing filter prior to sampling, we observe the increasing on the noise PSD inside the band of interest to evaluate the equivalent aliasing factor. Differently from equation (3-13), the actual filtering function is applied and the aliasing factor is not for a simple scalar anti-aliasing Δn, but the filter response along the frequency. Differently from (3-50), the generated sampler noise is calculated referred to the output in order to avoid the aliasing noise of the block itself, where the gain of the process is considered:

$$PSD_{ng} = Gv \cdot \left[4 \cdot \psi^2 \cdot K \cdot T \cdot R \cdot (F-1)\left(V^2/Hz\right)\right] \tag{3-64}$$

In the DT domain representation, the output spectra are considered from -fs/2 to fs/2, which is not the case in the operation of (3-63), which has a period of fs but a CT spectrum. Like in the filtering process, the decimation is better implemented in the frequency domain, in order to accelerate the simulation time. The decimation in this case is simply forcing to zero the spectrum beyond -fs/2 and fs/2. DT blocks following the sampler are also implemented with this technique. The spectra and functions are defined considering the wide spectrum, and then the output spectrum is defined within the band -fs/2 to fs/2.

5 Conclusion

The context of DT architectures and BPS process push the need for an innovative system level approach. Another constraint regarding the optimization of power consumption motivates the study towards a system level approach which discriminate the contribution of the different blocks on the whole chain and also quickly test various distributions of constraints. Using this approach, we compare the block performances in various configurations to the performances of the state of the art. This clarifies critical block specifications, both in performance and power consumption, and enables the redistribution of the constraints to optimize power consumption. The particular phenomenon of spectrum aliasing related to BPS architectures leads to non-classical system level design and modeling, notably on the wideband frequency domain system level simulation.

The various requirements over the system level analysis, intrinsic to the BPS process, such as wideband aliasing noise, motivate the development of a system level simulation tool in

which the figure of merit is a local SNDR evaluation in the band of interest. Another advantage of the tool is the vector processing and hybrid frequency / time domain calculation, which enhances the accuracy and time of the process. The building blocks are modeled for different types of input signals (noise, distortion, signal of interest). In order to separate the different types of signal in a non-linear transfer function, the Bussgang theorem is applied, which allows to accurately evaluating the resulting SNDR in a band of interest. In CHAPTER 6 it will be used on the impact of phase noise on local SNDR in the mixing and BPS processes. The proposed method and simulation tool are applied on the next chapter in order to evaluated and validate different types of BPS architectures in the ULP RF standards context. The analysis of three different BPS architectures based on the literature is conducted thanks to the proposed methodology. This leads the definition and specifications of an innovative architecture, which demonstrates an optimal trade-off in our context.

APPENDIX A THE SYNCHRONIZED/COHERENT SAMPLING

Consider s(t) a periodic signal with period T_S, sampled at constant period $1/T_{res}$, and that the Nyquist-Shannon criterion is satisfied. If N samples are considered, the sampled signal is defined by:

$$p(t) = s(t) \cdot g(t) \tag{3-65}$$

$$g(t) = \sum_{k=0}^{N-1} \delta(t - kT_{res}) \tag{3-66}$$

where g(t) is a finite sequence of N Dirac pulses. The Fourier Transform P(f) is the convolution between S(f) and G(f)

$$P(f) = S(f) * G(f) \tag{3-67}$$

$$G(f) = \frac{\sin(\pi f T_{res} N)}{\sin(\pi f T_{res})} \cdot e^{-j\pi N T_{res} f} \tag{3-68}$$

G(f) is equal to zero for $f_0(k)=k/(NT_{res})$, for k integer and different from multiples of N. G(f) is periodic, and because of (3-67), P(f) is also periodic. Calculating P(f), it gives:

$$P(f) = \sum_{k=0}^{N-1} s(kT_{res}) \cdot e^{-j\pi f k T_{res}} \tag{3-69}$$

Consider the DFT of p(t), where $T=N \cdot T_{res}$:

$$P\left(\frac{n}{T}\right) = \sum_{k=0}^{N-1} s(kT_{res}) \cdot e^{-j\pi k n/N} \tag{3-70}$$

When $T=T_s$ (synchronous sampling), G(f) has zero values situated at frequencies equal to the harmonic frequencies of s(t), the main lobe of G(f) attains its peak value for frequencies $f = n/Ts$, $0 \le n \le N-1$. $P(n/T_s)$ of P(f) are equal to the harmonics components of s(t).

Whenever $T \neq Ts$, all harmonic components give a non-zero contribution in the evaluation of the n^{th} harmonic component. This harmonic interference depending on both S(f) and G(f) is responsible for the "long-range leakage" which affects the measurement of S(f).

APPENDIX B THE BUSSGANG THEOREM AND THE APPLICATION IN THE FREQUENCY DOMAIN

According to the Bussgang theorem [107, 108], the corresponding output signal from a zero-memory non-linear system given by an attenuated version of the input signal plus a statistically independent to the signal error term, a non-correlated to the signal distortion D. The distorted signal at the output can be written as:

$$v_{out} = Gv \cdot v_i + A \cdot v_i + D \tag{3-71}$$

$$\alpha_3 \cdot v_i^{\,3} = A \cdot v_i + D \tag{3-72}$$

v_{out} contains the linear amplified version of v_i , a correlated portion of vi, where A represents the saturation of the signal, and D the uncorrelated part of the signal. The Bussgang theorem states that the covariance of a Gaussian stationary process (in our case v_i) and of its version passed trough a zero-memory non-linearity (in our case $\alpha_3 \cdot v_i^3$) is proportional to the variance of the process:

$$A = \frac{\mathrm{E}\left\{\left(v_i^{\,*}\right)\left(\alpha_3 v_i^{\,3}\right)\right\}}{\mathrm{E}\left\{\left(v_i^{\,*}\right)\left(v_i\right)\right\}} \tag{3-73}$$

The cross-correlation function between two variables f(t) and g(t) is by definition defined as:

$$h(\tau) = \int_{-\infty}^{\infty} f^*(t)\, g(t-\tau)\, dt \tag{3-74}$$

Since we consider a zero-memory system we observe h(t) for $\tau=0$, which actually applies for the covariance between f and g, therefore the covariance is given by:

$$h(\tau)\big|_{\tau=0} = \int_{-\infty}^{\infty} f^*(t)\, g(t)\, dt \tag{3-75}$$

The expression (3-75) is by definition the *Inner Product* space between g and f:

$$\langle f, g \rangle = \int_{-\infty}^{\infty} f^*(t)\, g(t)\, dt \tag{3-76}$$

And from the Parseval's theorem, the *Inner Product* space is also defined in frequency domain:

$$\langle f, g \rangle = \int_{-\infty}^{\infty} F^*(f)\, G(f)\, df \tag{3-77}$$

To calculate the A parameter of (3-73) is given as follows:

$$A = \frac{\left\langle v_{in}, \alpha_3 \cdot v_{in}^{\,3} \right\rangle}{\left\| v_{in} \right\|^2} \tag{3-78}$$

This in the frequency domain gives:

$$A = \frac{\int_{-\infty}^{\infty} V_i^*(f) \cdot \alpha_3 V_i^{\,3}(f)}{\int_{-\infty}^{\infty} V_i^*(f) \cdot V_i(f)} \tag{3-79}$$

This inner product is defined for a complete metric space, we are interest in a *Finite Metric Space* which is defined in frequency domain considering the interval f [f1,f2]:

$$A = \frac{\int_{-f1}^{f2} V_i^*(f) \cdot \alpha_3 V_i^3(f)}{\int_{-f1}^{f2} V_i^*(f) \cdot V_i(f)} \tag{3-80}$$

This means that we calculate the covariance of filtered versions of $v_{in}(t)$ and $\alpha_3 \cdot v_i^3(t)$ in the band of interest [f1,f2]. We redefine (3-73) inside f [f1,f2], meaning that $A_{[f1,f2]}$ is calculated in frequency domain:

$$A_{[f1,f2]} = \frac{\left\langle v_{in}, \alpha_3 \cdot v_{in}^3 \right\rangle_{[f1,f2]}}{\left\| v_{in} \right\|^2_{[f1,f2]}} \tag{3-81}$$

This definition shows that the proportionality factor A can be calculated either in the time or frequency domain, which is important for us since $A_{[f1,f2]}$ will be calculated in the frequency domain in the system simulation tool

Chapter 4 : Quantitative Comparison and Definition of a Bandpass Sampling RF Receiver

1 Introduction

The aim of this chapter is to compare various BPS architectures applied on the ULP RF standards: BT-LE and IEEE802.15.4. A system level design is implemented for such comparison. We concentrate the effort on developing the different filtering and frequency plan techniques, and, in addition, we define required features such as agility, level of integration and power consumption. Various sampling frequencies, signals to be sampled, center frequencies and sampling capacitances set the different trade-offs of BPS presented in CHAPTER 2 and will be applied on the various architectures on this chapter.

The architecture families defined in CHAPTER 2 are studied while applying the system level design methodology of CHAPTER 3. The figure of merit is the output SNDR inside the band of interest. From this study we compare the critical blocks defined for each configuration. Furthermore, a novel BPS architecture is proposed merging the best characteristics found amongst these three architectures. This architecture has been patented during this Ph.D. ([109]).

In CHAPTER 2 has been defined a classification of the DT architectures based on the state of the art and three main families have been retained: the Nyquist-Like Sampling, the RF/IF Bandpass Sampling with single path filter and the RF/IF Bandpass Sampling with complex filtering. The Nyquist-Like Sampling implements direct conversion while applying high sampling frequencies ([2]). This architecture is presented and specified for the ULP RF standards in section 2. The RF/IF Bandpass Sampling with single path filters reduces the sampling frequency while applying voltage sampling. In section 3 we present the complex sampling configuration similar to ([20]), and section 4 presents the use of CT IF filter for anti-aliasing and image rejection, thus applying single path sampling.

The concept of complex filtering is presented in [17, 18] and is the third family presented in CHAPTER 2. Section 5 presents a novel BPS architecture which merges the high under-sampling ratio of the second family using a first *IF1* close to the RF, and the Low-IF before demodulation using complex DT filtering of the third family for image and interferer rejection. The frequency plan, filtering functions and block specifications are derived for the proposed architecture.

2 ↑*fs* and ↑*f0* : The Nyquist-Like Sampling

2.1 Architectural Description

The direct conversion charge sampling architecture is used with DT receivers on [4, 15, 16, 43]. Figure 4-1 illustrates the configuration of this architecture designed for the proposed application. In the case of a wideband multi-standard receiver, the LNA has to cover a wide range not only regarding the frequency domain, but also considering power dynamic range, demanding highly linear LNA. Our application covers only the 2.4GHz ISM band, relaxing the LNA constraints. While using an RF front-end filter, a moderate- to low-linear LNA can be applied.

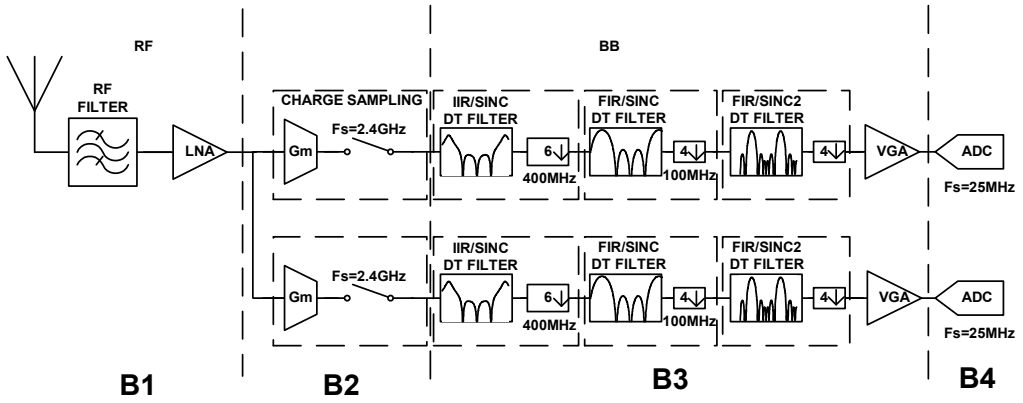


Figure 4-1 : Zero-IF Charge Sampling Block Diagram

The gain prior to sampling allows reducing the impact of the KT/C noise (CHAPTER 2) in terms of SNDR degradation. Two transconductance amplifiers convert the signal into current in order to implement a quadrature charge sampling. The signal is down-converted to zero- or low-IF. We remind from (CHAPTER 2) that the charge sampling integrates the input voltage over an interval of time, which represents a convolution by a window, i.e. a filtering function prior to sampling.

On the BPS sampling process, the wideband spectrum is folded into the Nyquist band (CHAPTER 2). The aliasing of the LNA output noise is filtered out by this integration window. On the other hand, the sampling frequency can not be reduced as in classical voltage BPS process, because the integration filter would also reject the signal of interest itself. (Figure 12 from CHAPITER 2). As a matter of fact, fs is in the same order of magnitude of f_{RF} or higher. The high center frequency to be sampled $f_0=f_{RF}$ pushes the constraints in terms of the *Gain Bandwidth* (G·BW) product of the sampling system.

The positive point of sampling at high frequencies is that the KT/C noise is distributed in a wider band, therefore, reducing the PSD (equation 27 CHAPTER 2). The anti-aliasing filter and the low sampler PSD relax the constraints on the LNA gain. Although the signal information occupies a narrow band after down-conversion, the front-end speed is dictated by fs. This means the blocks cut-off frequency after the sampler should comply with the frequency rate of 2·fs.

In a SDR context, the ADC sampling frequency is as high as the first applied sampling frequency, f_{ADC}=fs. The specifications of such ADC are impractical in a low power context. In our case, a reasonable ADC sampling frequency should be way below the first sampling frequency, f_{ADC}<<fs; to that purpose, decimation stages are employed. DT filtering is used to avoid unwanted aliasing (Figure 4-3). The next section presents how the frequency plan implements this high decimation order. The DT filters applied prior to the ADC are implemented in the continuous amplitude domain, i.e. analog. These techniques are of great interest in that case. The block implementing such function is the switched capacitor network. The basic principle is the charge sharing. The DT analog filter implementation and theory are explained in CHAPTER 5.

As presented in CHAPTER 2, not only the wideband noise aliases into the band of interest, but also in-band interferers. If the distance of the interferer with regards to the signal of interest is the same than the sampling frequency or one of the decimated frequencies, the interferer falls into the band of interest. The required in-band interferer rejection is defined in CHAPTER 3.

Since charge sampling architectures present a high decimation factor, the filtering and decimation are implemented in multiple stages. This technique is known in digital signal processing as successive decimation. At the end, the cascaded DT filtering frequency response may not be enough to implement channel selection, but only anti-aliasing. In this case, the close-in interferer (adjacent and alternate channel) represents the strongest signal at the ADC input (in the maximum gain mode). The ADC dynamic range, and therefore the effective number of bits n_{beff}, must be dimensioned accordingly. A VGA completes the remaining gain needed to fit to full-scale on the ADC input. On the following section we derive the frequency plan and the filtering functions for the architecture of Figure 4-1 for the ULP RF standards.

2.2 Filtering Techniques & Frequency Plan

In order to define the interferer rejection required for the standards, we remind the specifications of the ULP RF standards of CHAPTER 3. In (equation chapter3) is defined the required interferer rejection prior to aliasing process:

Parameter	IEEE802.15.4	BT-LE
In Band Interferer rejection	36.5dB	44dB
Image rejection	not specified	26dB

Table 4-1 : The proposed receiver frequency plan for fixed IF1

In the case where zero-IF conversion is used, the aliasing image is not a problem. On the other hand, *In- and Quadrature-phase signals* (I/Q) amplitude and phase mismatches lead to signal distortion, thus increase the EVM. In the case where the low-IF conversion is used, the signal down-conversion to base band and image rejection is implemented by a modified Weaver structure [110]. The I/Q mismatches lead to a limitation on the image rejection Δ_{int} [97]

$$\Delta_{im} = \frac{(1+\varepsilon)^2 - 2(1+\varepsilon)\cos(\Delta\theta) + 1}{(1+\varepsilon)^2 + 2(1+\varepsilon)\cos(\Delta\theta) + 1} \quad (4\text{-}1)$$

where: ε : $(G_I - G_Q)/G_I$ the relative gain mismatch and Δθ the phase mismatch. The required Δim=26dB by the following combination of ε and Δθ (figure):

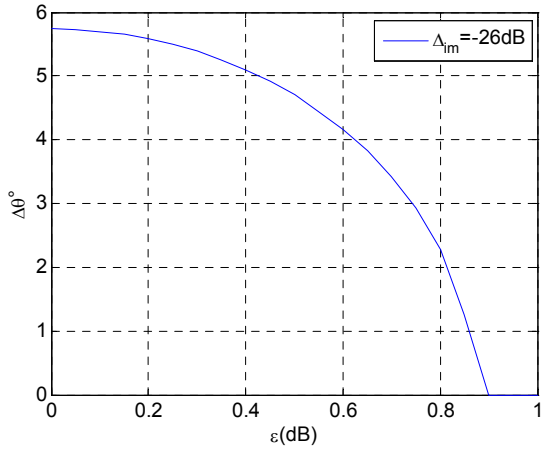


Figure 4-2 : Maximum gain and phase mismatch requirements for Δ_{im}=26dB

The lowest sampling frequency sets the aliasing in-band interferer potential frequencies. In this case, the maximum f_{ADC} (Figure 4-3) is set considering a power consumption criterion. From the state of the art of CHAPTER 2 and considering the data base of [82], it is inferred that a low power ADC complies with sampling frequency under 25MSPS and a n_{beff}=6bits. For those performances, a ADC power consumption P_{ADC} under 1mW is achievable. Considering the application of such ADC in Figure 4-1, a high decimation ratio N=96 is needed between fs to f_{ADC}. The decimation filters are a combination of DT *Finite Impulse Response* (FIR) and DT *Infinite Impulse Response* (IIR) filters. In Figure 4-3 is summarized the filtering and down-conversion steps.

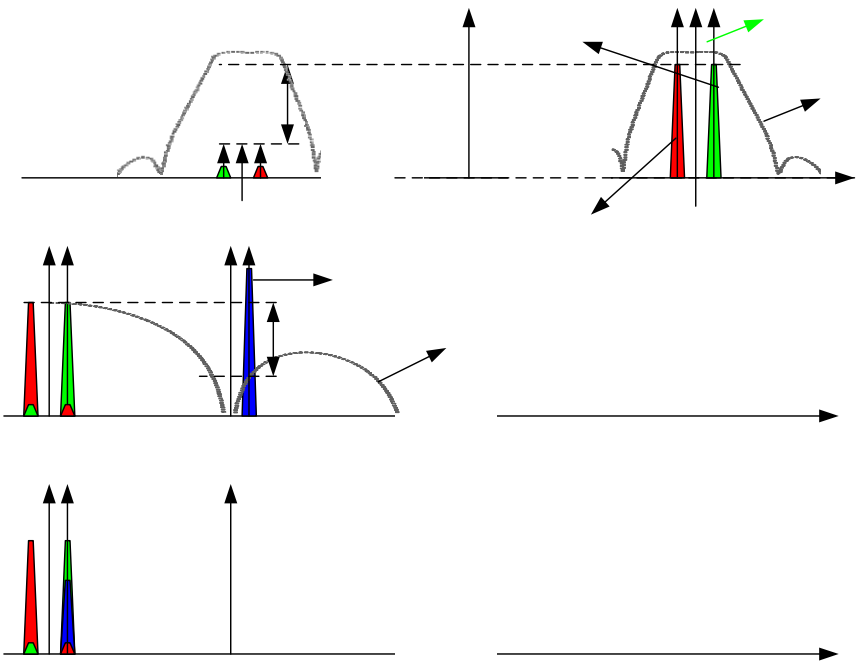


Figure 4-3 : The down-conversion and filtering on the architecture of Figure 4-1

As defined in Table 4-1, in-band interferers situated at multiples of f_{ADC} (in our case 25, 50, and 75 MHz) from the signal of interest, must be rejected by 44dB. To achieve such rejection, we propose a cascade of decimation filters. The first DT is an IIR transfer function. The filter is simplified since the only objective is the wideband noise anti-aliasing. The frequency response is illustrated in Figure 4-4. The decimation order is 6. The second filter is a FIR, followed by a decimation ratio by 4 (Figure 4-5). The third filter, which precedes the in-band interferer aliasing, implements a FIR/$Sinc^2$ frequency response. The $Sinc^2$ frequency response means that the order of the filter is twice the decimation order [4]. As explained in CHAPTER 5, the filters obtained using only charge sharing discharge the capacitors on the output. In order to have a filter order higher than the decimation order, either active blocks are used or samples go to two different paths, doubling the charge, therefore attenuating the signal [4]. After decimation, the cut-off frequency of active blocks is reduced; therefore it is more interesting to apply further gain after the filter (passive network + amplification) in terms of power consumption. In the filter illustrated in Figure 4-7, a gain is applied after sampling to compensate the losses of a passive filter. In this application where low IF is aimed at, an IIR filter is not applicable since its selectivity would reject the signal of interest itself [79]. The resulting frequency response of the $Sinc^2$ filter is illustrated in Figure 4-6 and the cascaded is illustrated in Figure 4-7.

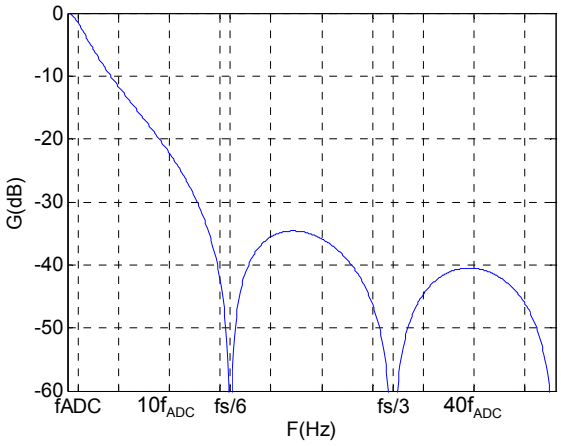


Figure 4-4 : First DT filter frequency response

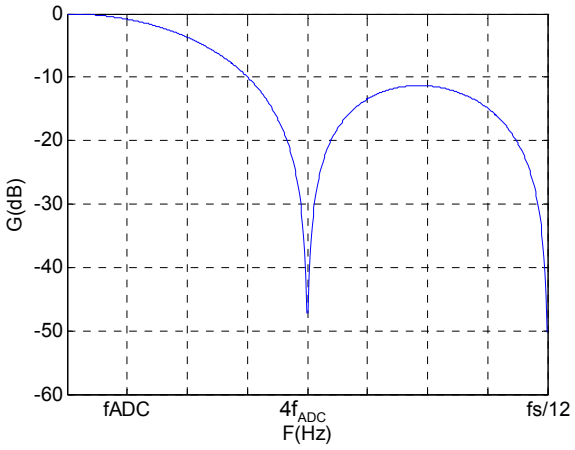


Figure 4-5 : Second DT filter frequency response

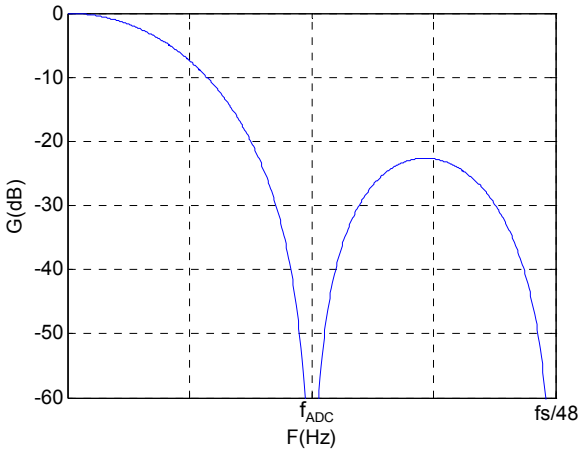


Figure 4-6 : Third DT filter frequency response

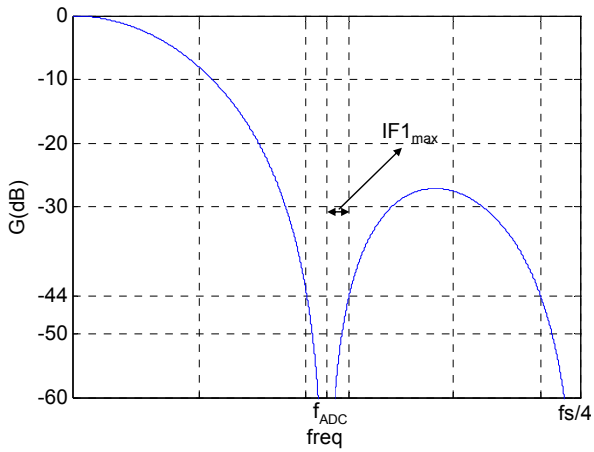


Figure 4-7 : Cascaded DT filter frequency response

Since the decimation factor is fixed at 96 but f_{RF} varies from 2.4GHz to 2.48GHz, f_{ADC} also varies from 25MHz to 25.883MHz. On the other hand, the digital base band blocks need to work in a single frequency. In this case, digital DT filters can be designed to implement channel selection, which is proceeded by non-integer decimation algorithms [7]. From the filtering function of Figure 4-7 we find the highest possible low-IF, $IF1_{max}$. It is defined by the highest distance from f_{ADC} for which Δ_{int}=44dB is still respected, in this case low IF=2.3MHz.

2.3 System Level Design and Validation

The next step in the system level consists in defining the aliasing factor γ for each block of the receiver. The blocks in question are the sampler and the decimation filter network. We have presented in CHAPTER 2 that the charge sampling integration filter depends on the integration time interval, therefore on the applied duty cycle. Applying fs=f_{RF} with a duty cycle of 0.5 leads to the equivalent filter acting as a Sinc function with zeros at 2·m·fs (m=1, 2, 3,). The aliasing factor is obtained through the system level simulation tool applying the Sinc filter. The resulting aliasing factor is γ=4.21. This means that the SNR_{deg} for the block B2 of Figure 4-1 will be at least SNR_{deg_dB}=6.25dB.

Another information about the receiver is the target ADC specification at n_{beff}=6bits and f_{ADC}=25MSPS. Considering an ADC topology which presents a flat quantization noise, we find the equivalent $NF_{ADC\_50\Omega}$=69.1dB (equation of chapter 3). The calculated NF is the starting point to define the SNR degradation distribution and the gain applied prior to the ADC. Considering the building blocks performances from the state of the start presented in CHAPTER 2, the results for the aliasing factor and NF_{ADC}, the SNR and SNDR degradation distributions are calculated. Considering the method presented in CHAPTER 3, the antenna impedance Z_{ant} defines the input voltages (signal of interest, noise, interferer, intermodulation product). The evolution of the interferers in the IIP3 test bench considers the receiver nominal gain and the interferer rejections obtained in Figure 4-7. For the maximum gain calculation, the strongest interferer test bench P_{int_max} is found, then the maximum ADC input dynamic range and, if there is adjacent channel filtering, the possible adjacent rejections. Table 4-2 summarizes the receiver parameters able to define the total gain:

	Parameter	Value
Front-end Conditions	Z_{ant}	50 Ω
	V_{p_p}	1V
	P_{ADC_max}	21dBmV²
BlueTooth Low Energy	P_{int_max}	-23dBmV²
	Δ_{adj}	0dB
	Gv_{max}	44dB
IEEE802.15.4	P_{int_max}	-35dBmV²
	Δ_{adj}	0dB
	Gv_{max}	56dB

Table 4-2 : Summary of the block specifications for the architecture in Figure 4-1

After deriving all blocks specifications through the system design method, the blocks fine specification tuning is done using the system level simulation tool. The block specifications are summarized in Table 4-3. The receiver architecture is separated in active macro blocks from B1 to B4. The maximum sampling capacitance is limited by the front-end cut-off frequency and required "gm" to drive this capacitance at the input f_{RF} frequency. Considering (eq.23 from CHAPTER 2) for the charge sampling system, Cs=0.4pF in order to have 0dB @ f_{RF} for gm=3mS ($\Delta t \cdot fs=0.5$). The sampling thermal noise PSD, defined by fs and Cs, (eq. 26 CHAPTER 2 [13]) generated by the sampler is -137.6dBmV^2/Hz, resulting in an equivalent 50Ω noise figure of 16.4dB. The allowed noise figure for B3 consisting of the filtering network and the VGA depends on the sampler gain. Although the signal is down-converted to base band, the sampling frequency is still $fs=f_{RF}$ which pushes the sampler gain power consumption.

Standard	Parameter	B1	B2	B3	B4	TOTAL
Bluetooth Low Energy	Gv (dB)	10	10	24	0	44
	SNR_{deg}(dB)	12.4	6.8	4.5	5.3	29
	γ	1	4.21	1	1	-
	$NF_{50\Omega}$(dB)	12.4	20	41.8	71.5	-
	$SNDR_{deg}$(dB)	12.5	7.2	6	9.3	35
	$IIP3_{50\Omega}$(dBmW)	-16.5	-12.6	-6.5	12.3	-
IEEE802.15.4	Gv (dB)	10	15	31	0	56
	SNR_{deg}(dB)	12	6.8	1.4	1.3	21.5
	γ	1	4.21	1	1	-
	$NF_{50\Omega}$(dB)	12	19.7	39.7	71.7	-
	$SNDR_{deg}$(dB)	12.1	7.2	2.4	2.8	24.5
	$IIP3_{50\Omega}$(dBmW)	-20.8	-17.6	-5.6	22.1	-

Table 4-3 : Summary of the block specifications for the architecture in Figure 4-1

In the maximum gain mode, there is no rejection of the strongest interferer @ Δf=3MHz, since the last decimation filter stage is a FIR type (Figure 4-7), which is not a selective filter. The decision of applying FIR response comes from the fact that low-IF is applied. In order to verify the filtering function derived in Figure 4-7, the system level simulation tool of CHAPTER 3 is applied. The DT filtering theory is detailed in CHAPTER 5. In Figure 4-8 is illustrated the spectra obtained from the simulation tool after the sampling process for a test bench consisting of the signal of interest and an interferer @ $\Delta f = f_{ADC}$ for BT-LE. From there, the signal is DT filtered and decimated successively. Figure 4-9 shows the spectra at the output of the last DT filter, and Figure 4-10 illustrates the spectra after decimation.

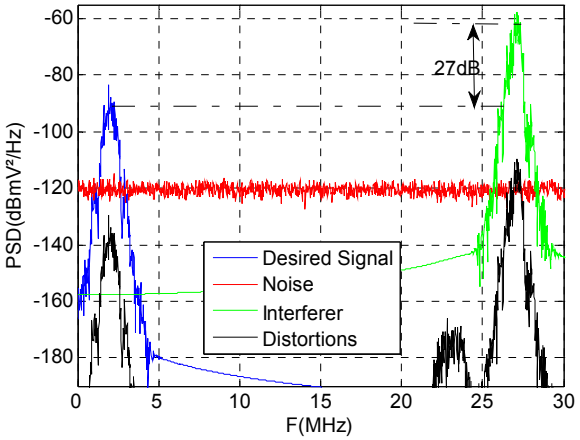


Figure 4-8 : The signal spectra after sampling

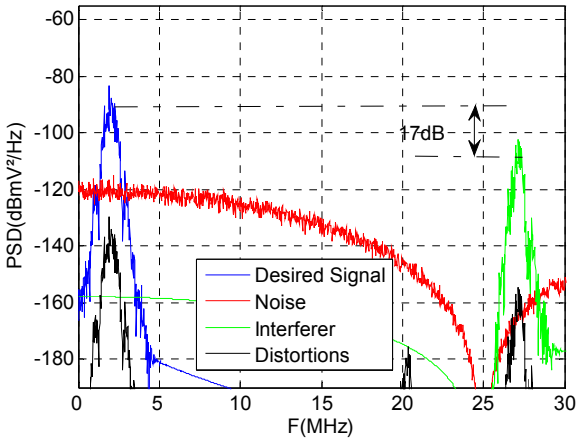


Figure 4-9 : The signal spectra after DT filtering

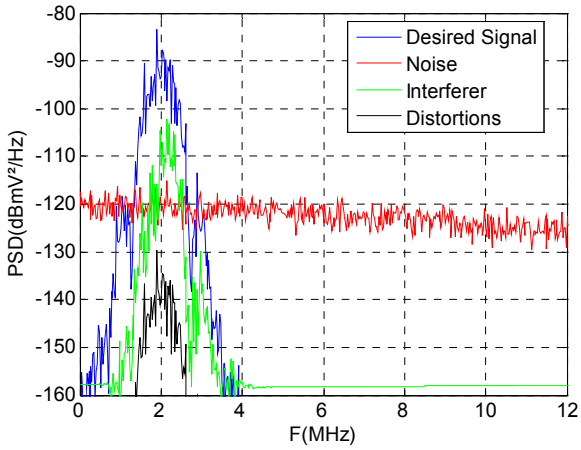


Figure 4-10 : The signal spectra after decimation

As set in the interferer profile of CHAPTER 3, the interferer PSD is 27dB above the signal PSD and, after the last DT filter, is 17dB below which represents the noise floor at the ADC output as well, validating therefore the filter for the application on the ULP RF standard. Considering the aliasing frequencies identified in 2.2 and the interferer profile defined in CHAPTER 3, Table 4-4 summarizes the resulting simulated SNDR for the critical test benches:

Standard	Test Bench	SNDR(dB)
Bluetooth Low Energy	Sensitivity	14.2
	Int @ Δf=25MHz	14.6
	Int @ Δf=50MHz	17
	Int @ Δf=75MHz	17
	IIP3	14.3
IEEE802.15.4	Sensitivity	3.6
	Int @ Δf=25MHz	5.9
	Int @ Δf=50MHz	6.6
	Int @ Δf=75MHz	6.8
	IIP3	3.8

Table 4-4 : Summary of the simulated SNDR for in presence of interferers

In conclusion, whereas in this architecture the high sampling frequency means less noise for the sampler, the gain prior to the successive decimation processes has to run as fast as the sampling frequency fs=f_{RF}. Another drawback of the high sampling frequency is the DT filter complexity, which requires multiple stages. Since the DT filter must implement the in-band interferer rejection alone, a Sinc² frequency response is needed, which leads to a filter order twice the decimation order. The frequency synthesis represents another challenge since quadrature oscillator is needed at f_{RF}. We can used either a polyphase generation [111] or a reference at twice f_{RF} [2]; in both cases the sampler + decimation filter network is subjected to I/Q gain and phase mismatches. To avoid the zero-IF conversion which suffers from 1/f noise, DC offset and second order distortions, the signal is down-converted to low-IF on the sampling process, which leads to the use of a FIR filter instead of an IIR filter. The low-IF is limited by the filter showed in Figure 4-7, where the in-band interferer rejection is achieved in the f_{ADC}±2.3MHz range.

The obtained LNA and VGA performances lead to relaxed NF and IIP3 specifications, which are derived considering a given distribution obtained from the method of CHAPTER 3. In order to reduce the frequency synthesis constraint, but also frequency of the blocks after sampling, the technique of voltage sampling [112] (CHAPTER 2) is a potential solution. The next architecture is a configuration where a strong under-sampling ratio is employed and some anti-aliasing filtering techniques are used to overcome the drawback the spectrum aliasing.

3 ↓*fs* and ↑*f0*: RF BPS with quadrature sampling

3.1 Architectural Description

In the interest of reducing the sampling frequency on the system, but still addressing signals with high center frequencies, a high under-sampling ratio can be applied during the BPS process. The sinus cardinal filtering inherent to charge sampling becomes undesirable in this case. This technique relaxes the decimation filtering complexity and the frequency synthesis power consumption. This architecture is similar to [20] (Figure 4-11). The applied voltage sampling frequency is 25 times slower than for the previous architecture, in the range of BW_{RF}=80MHz. Decimation from fs to f_{ADC} is still required, but its order is strongly reduced, which represents a reduction on the DT filter complexity. On the other hand, the sampler PSD increases compared to the previous architecture if the same sampling capacitance is used (eq. 15 from CHAPTER 2).

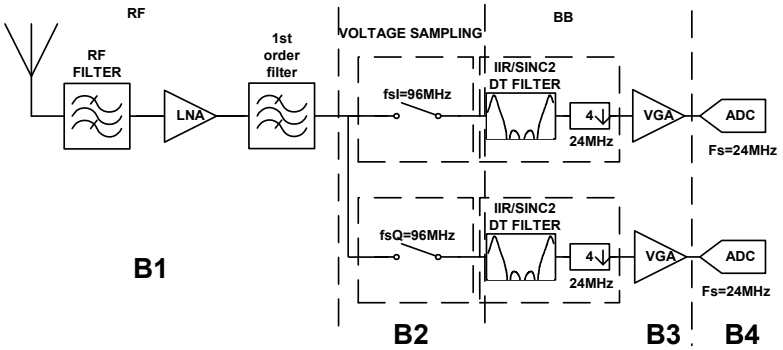


Figure 4-11 : Direct RF complex voltage BPS

Low linearity LNA is still used in this application to optimize power consumption. The application of a RF front-end filter presenting strong out-of-band rejection allows reducing IIP3 requirements at all levels but mostly on the LNA. The filter after the LNA is applied to reduce the aliasing factor γ compared to the previous architecture. A first order bandpass filter with bandwidth of BW_{RF} can be obtained using a tuned LNA ([18]). To show the trade-off between the use of a selective filter and applying low-IF architecture, we choose to apply selective filter and compare it to the previous architecture. A more selective IIR DT filter can be used in order to reduce IIP3 specifications of its succeeding blocks and the ADC dynamic range requirements.

The quadrature sampling is applied in this architecture. It is observed that the phase shift between the sequences of Diracs is accumulated over the frequency, which is an intuitive result since a constant time delay represents different phases for different frequencies. The I/Q mismatch is a strong limitation of such architectures considering the fact that the phase shift between the samplers cumulates over the harmonics. As defined for the architecture of section 2, the aliasing of in-band interferers into the band of interest is the most constraining point for the filtering specifications. In this case, a DT decimation filter is applied prior to the VGA that completes the gain for the ADC input. On the following sections we give the details on the filtering techniques, the frequency plan and the blocks specifications. Strong and weak features of this architecture appear from the resulting required performances on the ULP RF standards.

3.2 Filtering Techniques & Frequency Plan

The architecture presented in Figure 4-11 has just one down-conversion, and the RF filter presents the same bandwidth than the standard BW_{RF}, therefore only filter out-of-band signal and not in-band-interferer. In this case, in order to avoid in-band interferer aliasing after the sampling process, the sampling frequency is above the RF bandwidth, $fs>BW_{RF}$. In Figure 4-12 we illustrate the cases for the demodulation of the first or the last RF channel, we observe the harmonics of the sampling frequency and the aliasing bands and the fact that it falls outside the RF frequency. We remind from CHAPTER 3 the ULP RF standards bandwidth of BW_{RF}=80MHz.

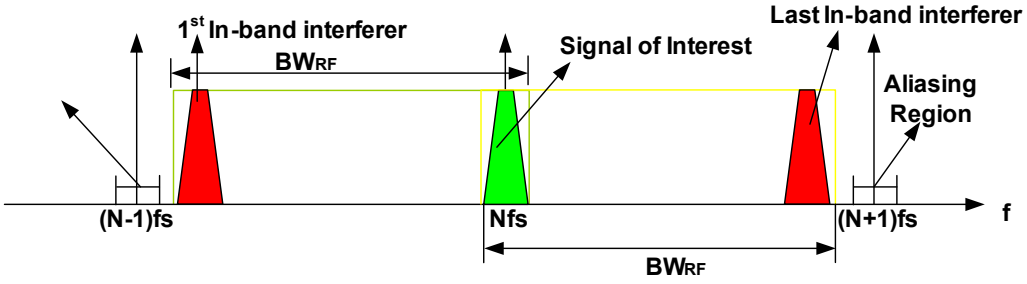


Figure 4-12 : The sampling frequency condition for non in-band interferer aliasing

At the ADC level, as presented in 2.2, a sampling frequency $f_{ADC} \approx$ 25MSPS and a resolution of Nb_{eff}=6bits are compatible with a low power implementation. Thereby, to achieve fs>80MHz, the minimum decimation order is M=4.

A third consideration to correctly set fs is the phase shift difference between fs_I and fs_Q. Presented in the state of the art of CHAPTER 2, the complex sampling is obtained by phase shifting the I and Q samplers. Consider I/Q phase shift as ϕ=90°, the n^{th} harmonic present ϕ=n·90° phase shift. If n is even, ϕ will be a multiple integer of 180°, meaning no distinction between I and Q signals. In conclusion, odd harmonics are needed for quadrature down-conversion. These three requirements lead us to choose fs=96MHz which corresponds to $fs=f_{RF}/25$. To address the 2.4GHz - 2.48GHz band, fs will vary from 96MHz to 99.2MHz, and f_{ADC} from 24 - 24.8MHz. The system requires a 40kHz frequency step to address a frequency step of 1MHz at f_{RF} allowing demodulating both IEEE802.15.4 and BlueTooth-LE channels.

The in-band interferer aliasing occurs at the decimation level, like for the previous architecture (Figure 4-3). The required interferer rejection is Δ_{Int}=44dB, defined in Table 4-1 at multiples of f_{ADC}. The DT filter of Figure 4-11 is implemented through charge sharing technique and switched-capacitor blocks [18]. In order to achieve the required rejection around the aliasing frequencies (multiples of f_{ADC}) and IIR/Sinc² filtering function is needed. The application of a selective IIR filter is this time possible since zero-IF is adopted in the architecture of Figure 4-11. The theory concerning the DT filtering is detailed in chapter 5 and the DT frequency response for this architecture is illustrated in Figure 4-13. As observed, the required rejection is attained for a BW of 4.5MHz around f_{ADC} and fs/2; considering the BT-LE BW_{ch}=1.25MHz, the filter easily respects the specifications.

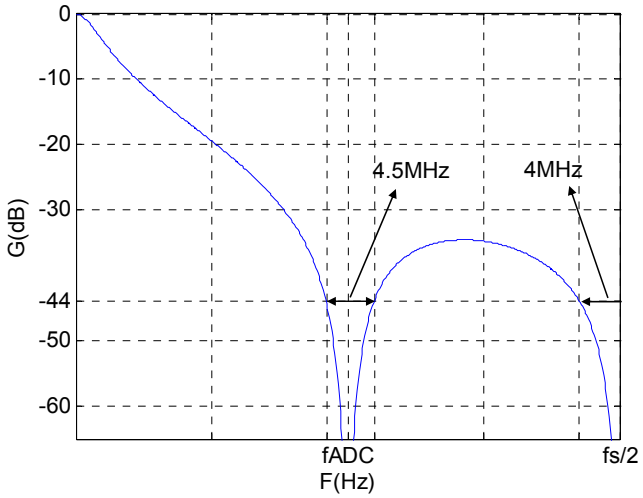


Figure 4-13 : DT filter of Figure 4-11 (B3) frequency response

3.3 System Level Design and Validation

As defined for the previous architecture, we first have to calculate the aliasing factor on the receiver of Figure 4-11. In this architecture, the sub-sampling ratio is $2 \cdot f_{RF}/fs$=50. From CHAPTER 2 the aliasing factor does not depend on the signal center frequency, in this case f_{RF}, but on the equivalent noise bandwidth BW_{Neq}. In this application, it is limited by a first order filter which bandwidth is BW_{RF}=100MHz (the tuned LNA output filter from Figure 4-11). It was presented in CHAPTER 2 that the equivalent noise bandwidth for a first order system is $BW_{noise}=\pi \cdot fc$, fc is the cut-off frequency of the first order system. The calculated aliasing factor is

γ=1.6, and applying the system simulation tool the resulting aliasing factor is γ=1.82. The last used as reference for the SNR degradation distribution.

The signal to be sampled is still at f_{RF} which leads to the same constraint in terms of "gm" than the previous architecture. Considering the same Cs=0.4pF as in the previous architecture, the S/H noise from CHAPTER 2 and fs=96MHz, the sampler NF referred to 50Ω is $NF_{S/H}$=30.4dB, which pushes the constraints on the LNA gain or on the subsequent blocks NF. The system design method is applied considering the sampler higher NF, and optimized through the system simulation tool. The results are summarized in Table 4-5. The reduction on the aliasing factor compared to the first architecture is due to the application of the tuned LNA, and it relaxes the S/H_{NF}. An allowed S/H_{NF}=32.1dB is set. This means that the same sampling capacitance can be used in this application, and that the increase of the sampler NF does not impact the total SNR degradation. Notice that contrarily of what was predicted, the LNA gain is not impacted as well.

The application of an IIR filter in the DT filter relaxes the constraints for the ADC level, the allowed NF_{ADC}=76.5dB means an effective number of bits of N_{beff}=5bits, 1bit less compared to the previous architecture. As it is presented in CHAPTER 5 the IIR filtering function is obtained just after the VGA, which implies that the VGA IIP3 is not relaxed by the selective DT filter. The ADC IIP3 also benefits from the IIR transfer function.

Standard	Parameter	B1	B2	B3	B4	TOTAL
Bluetooth Low Energy	Gv (dB)	12	10	27	0	47
	SNR_{deg}(dB)	12.6	8.8	2.3	5.3	29
	γ	1	1.82	1	1	-
	NF 50Ω(dB)	12.6	32.1	41.8	76.5	-
	$SNDR_{deg}$(dB)	13	9.2	3.5	9.3	35
	IIP3 50Ω(dBmW)	-19.7	-13.5	-6.6	10.2	-
IEEE802.15.4	Gv (dB)	16	10	35	0	61
	SNR_{deg}(dB)	13.1	5.8	1.3	1.3	21.5
	γ	1	1.82	1	1	-
	NF 50Ω(dB)	13.2	32.1	40.3	76.5	-
	$SNDR_{deg}$(dB)	13.5	6.2	1.5	3.3	24.5
	IIP3 50Ω(dBmW)	-24.4	-12.4	-2.2	14.4	-

Table 4-5 : Summary of the block specifications for the architecture in Figure 4-11

The use of the system simulation tool enables to validate the filtering and frequency plan techniques, and to verify the required SNDR for the different test benches. It is particularly interesting to display the in-band interferer rejection process. In Figure 4-14 and Figure 4-15 are illustrated the signal spectra before and after DT filtering, respectively. Figure 4-16 illustrates the spectra after decimation. Notice that the aliased interferer is far from the noise floor indicating

that the required rejection is attained with considerable margin (54dB rejection observed on Figure 4-14 and Figure 4-15).

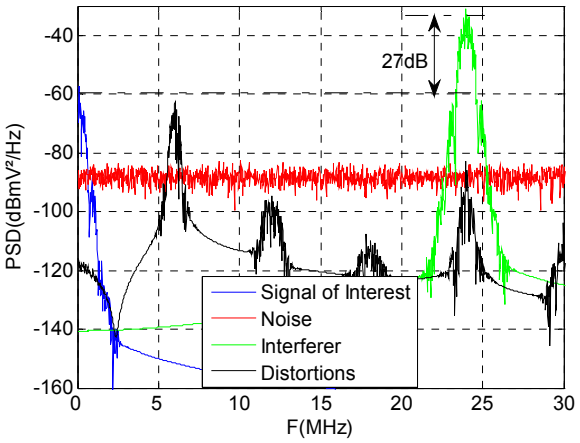


Figure 4-14 : The signal spectra after sampling

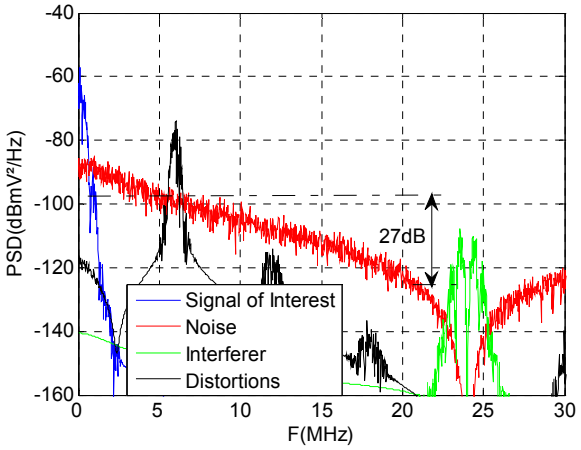


Figure 4-15 : The signal spectra after DT filtering

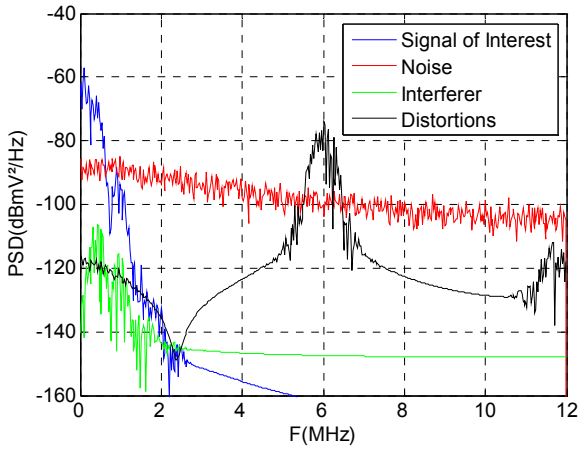


Figure 4-16 : The signal spectra after decimation

In Table 4-4 are summarized the resulting simulated SNDR for the identified critical test benches:

Standard	Test Bench	SNDR(dB)
Bluetooth Low Energy	Sensitivity	14.1
	Int @ Δf=25MHz	17
	Int @ Δf=50MHz	17
	Int @ Δf=75MHz	17
	IIP3	14.9
IEEE802.15.4	Sensitivity	3.5
	Int @ Δf=25MHz	6.4
	Int @ Δf=50MHz	6.7
	Int @ Δf=70MHz	6.8
	IIP3	3.6

Table 4-6 : Summary of the simulated SNDR for in presence of interferers

To conclude, this architecture lowers the sampling frequency and simplifies the DT filter implementation with no additional constraints on the LNA level, thanks to a more performing anti-aliasing filter. Compared to the previous architecture, the application of zero-IF brings back constrains such as 1/f noise, DC offset and second order distortions. The advantage is the possibility of using selective IIR DT filter, which relaxes the ADC linearity and dynamic range constraints. On the one hand, the I/Q mismatch at high under-sampling ratios is more constraining since the phase shift is accumulated over the harmonics. On the other hand, if compared in terms of delay, it represents the same delay as if $fs=f_{RF}$. Quadrature clock generation using $f_{OL}=2 \cdot fs$ and recombining phases, which is better in terms of mismatch performance, is eased when applying low fs.

Further simplification on the DT filter is intended since in this case the filter order is still twice the decimation order in order to respect aliasing in-band interferer rejection. If complex sampling / mixing is avoided, I/Q mismatch issues are strongly relaxed to a simple digital stage problem. In the following architecture, we discuss the possibility to apply selective anti-aliasing filter in IF level, in order to implement image and in-band interferer rejection.

4 ↓*fs* and ↓*f0* : IF BPS with Single Path Filtering

4.1 Architectural Description

The signal to be sampled in this architecture is no more centered at f_{RF}, but at a fixed intermediate frequency IF1 ([17, 19]). The main interest is to apply selective filtering prior to sampling and to apply single sampling frequency. Another positive point is the reduction of the sampler G·BW product with the reduction of the signal center frequency to be sampled from $f_0=f_{RF}$ to f_0=IF1. When applying the same sampling capacitance as for the previous architectures, the required "gm" is proportionally reduced with f_0. The proposed configuration for the IF BPS voltage sampling architecture is illustrated in Figure 4-17. The first questions to answer are: which technology can be used on the IF1 filter and which IF1 filter can be applied. From CHAPTER 2 we observed that to avoid using bulky SAW filters on the CT IF1 filter, compact filters based on LWR resonators are a very interesting upcoming technology. These filters can achieve very selective filtering performance (elliptic function) at center frequencies below 500MHz [72]. Another advantage of Lamb-wave technologies is the possibility to address high characteristic impedance, thus to reduce the constraints on the current driving the filter.

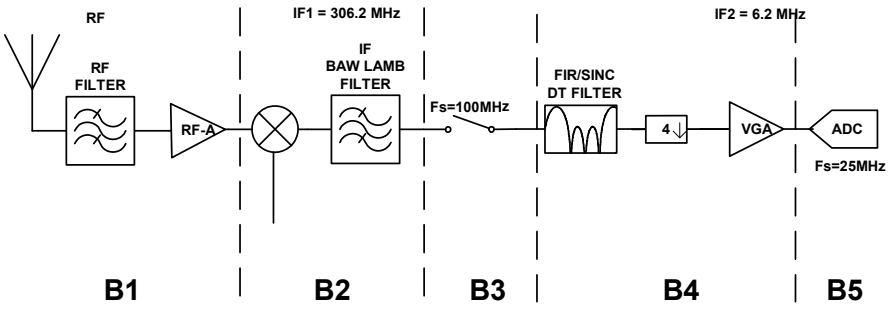


Figure 4-17 : IF Bandpass Sampling Block Diagram

The application of selective CT IF1 filter can reject the in-band interferers aliased at the decimation level (distanced from the signal of interest by multiples of f_{ADC} (Figure 4-3)) thus strongly relaxes, or perhaps even avoids, the use of DT decimation filters. In the example of Figure 4-17, a more conservative configuration is preferred where the aliasing in-band interferer rejection (Table 4-1) is shared between two CT filter / DT filter stages. Applying this technique, the DT stage can be strongly simplified compared to the previous architectures and the CT IF1 filter also has relaxed specifications. Contrary to the previous architectures, the above configuration uses single path for the down-conversion. On BPS process, the signal is down-converted to a low IF2. In this case, the image filter is implemented on the CT IF1 filter level. The highest reference frequency is lower than on the first architecture, but higher than on the second one since the mixer at f_{OL} increases as a low IF1 is aimed at. Although the frequency synthesis seems more complicated on this architecture than on the one from section 3.2, the advantage here is that no quadrature LO is needed.

4.2 Filtering Techniques & Frequency Plan

From (CHAPTER 2) the G·BW product is set for the voltage sampling. In this application, the lowest possible IF1 is targeted, but no assumption on the frequency synthesis block is made yet. The lowest possible IF1 applying LWR technology from the CT time filter point-of-view depends on a technology parameter called coupling coefficient (kt^2 as a % of the center frequency). This parameter links the filter bandwidth to its center frequency, and the required channel bandwidth BW_{CH}. The deriving of the lowest IF1 is detailed in APPENDIX C and is set as IF_{min}=250MHz, considering the technological parameters found the literature [72]. Regarding the down-conversion from f_{RF} to IF1, the image frequency IM_{RF} @ f_{IMRF} =f_{RF}-2·IF1 is filtered by the RF front-end filter since 2·IF1 is large enough against the RF filter bandwidth.

In the architecture of Figure 4-17, the CT IF1 filter is considered not to totally respect the aliasing in-band-interferer rejection Δint=44dB. As previously defined a sampling frequency higher than the RF bandwidth avoids in-band-interferer aliasing during the BPS process. Before setting the specifications for the CT IF1 filter, we observe the performance on the DT IF2 filter (Figure 4-18). Considering the applied ADC sampling frequency and resolution of the previous architectures and the fact that the digital demodulation is greatly simplified if f_{IF2}=f_{ADC}/4 ([1,0,-1,0] coefficients), we find f_{ADC}=25MHz and IF2=6.25MHz. Considering these conditions, the required sampling frequency is fs=100MHz, therefore the decimation order between fs and f_{ADC} is the same as the previous architecture, M=4.

The DT filter in Figure 4-17 implements a simple Sinc frequency response (Figure 4-18), where the filter order is the same than the decimation order and can be implemented by a fully passive network (detailed in CHAPTER 5). After sampling, possible in-band aliasing interferers are situated in 3·f_{ADC}/4, 5·f_{ADC}/4 and 7·f_{ADC}/4 (Figure 4-18). The resulting rejection is Δ_{int}=10dB. According to the required rejection (Table 4-1), 34dB are lacking for the interferer rejection, which is implemented prior to the sampling process on the CT IF1 filter level, at multiples of f_{ADC} away from IF1 (Figure 4-20). During the BPS process the signal is down-converted from IF1 to IF2=6.25MHz. A multiple of the sampling frequency defines the down-conversion to IF2:

$$IF2 = IF1 - N \cdot fs \tag{4-2}$$

From (4-2), considering the defined fs=100MHz and the lowest possible IF1=250MHz taking into account technology constraints, IF1 is set to 306.25MHz, and N=3 (Figure 4-20). Since no complex filtering is applied, the CT IF1 filter must be selective enough to reject the image frequency at f_{im}=IF1 - 2·IF2.

The proposed CT IF1 filter is based on piezoelectric resonators, and the implemented network is a second order lattice filter one (APPENDIX C). The filter frequency response and the required filtering mask are summarized in Figure 4-19. In order to verify the derived frequency plan and filtering functions and to conclude about the receiver performances, the architecture from Figure 4-17 is analyzed through the system level simulation tool.

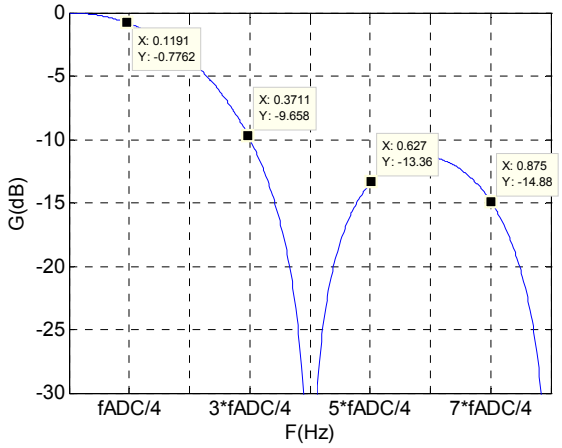


Figure 4-18 : DT filter frequency response

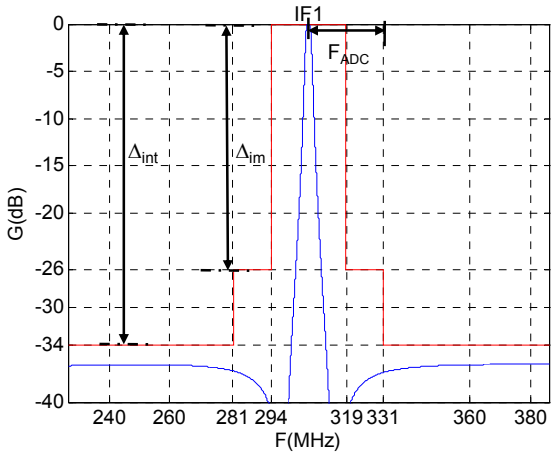


Figure 4-19 : The CT IF1 filter and mask

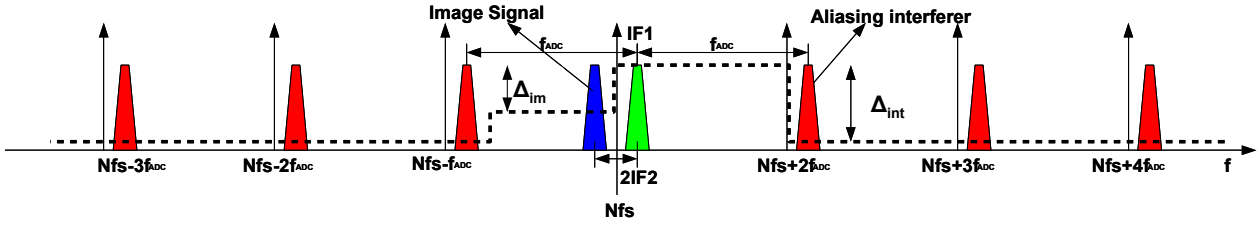


Figure 4-20 : The possible aliasing interferes and the image signal analyzed on *IF1* level

4.3 System Level Design

Since this sampling frequency architecture is quite similar to the previous one, the sampler NF is also similar; hence similar gain constraints are expected prior to sampling. On the other hand, the CT IF1 filter represents losses prior to sampling which are compensated by the mixer. Table 4-7 summarizes the block specifications:

Standard	Parameter	B1	B2	B3	B4	B5	TOTAL
Bluetooth Low Energy	Gv (dB)	12	0	10	28	0	48
	SNR_{deg}(dB)	13	3.4	5.6	2.6	4.4	29
	γ	1	2	1.6	1	1	-
	NF 50Ω(dB)	13	17.8	31.5	43.2	77	-

	$SNDR_{deg}$(dB)	13.5	3.9	5.7	4.5	7.4	35
	IIP3 50Ω(dBmW)	-20.4	-10.5	-34.2	-21.9	2.4	-
IEEE802.15.4	Gv (dB)	17	0	10	33	0	60
	SNR_{deg}(dB)	12.9	3.2	3.5	0.5	1.4	21.5
	γ	1	2	1.60	1	1	-
	NF 50Ω(dB)	12.9	19.3	31.2	37.5	76	-
	$SNDR_{deg}$(dB)	13	3.4	4	1.3	2.8	24.5
	IIP3 50Ω(dBmW)	-21.2	-7.5	-47	-43	-12.4	-

Table 4-7 : Summary of the block specifications for the architecture in Figure 4-17

On the previous architecture, the application of an IIR DT filter enables to reject adjacent interferers which limits the receiver gain and represents a constraint on the ADC dynamic range. On the previous architecture, the filtering block that allows to increase the total gain to Gv_{max_BT-LE}=48dB is the DT IIR filter. In this architecture, the DT filter is an FIR function, which is not selective. The CT IF1 filter alternatively implements a selective filtering (Figure 4-19), and Gv_{max_BT-LE}=48dB can still be used. In consequence, the same ADC n_{beff}=5bits can be kept. It is important to highlight that single path reception means half of the receiver blocks from the sampler to the ADC.

On the following, we illustrate how the interferer rejection is implemented in two stages before aliasing into the band of interest while the required SNDR is kept. Figure 4-21 and Figure 4-22 show the signal spectra before and after the CT IF1 filter, and Figure 4-23 and Figure 4-24 show the signal before and after DT filter. The chosen test bench is the down-conversion of the first channel for BT-LE in the presence of an interferer @ $\Delta f=3\cdot f_{ADC}$=75MHz.

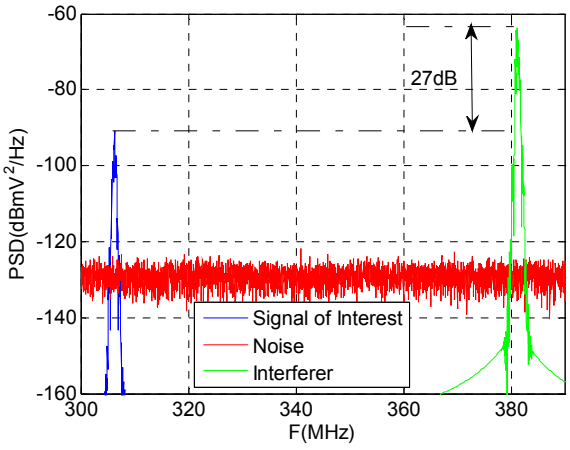


Figure 4-21 : The signal spectra after mixing

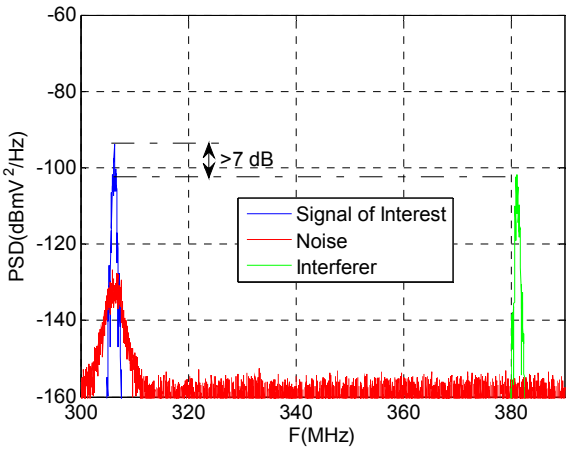


Figure 4-22 : The signal spectra after CT filtering

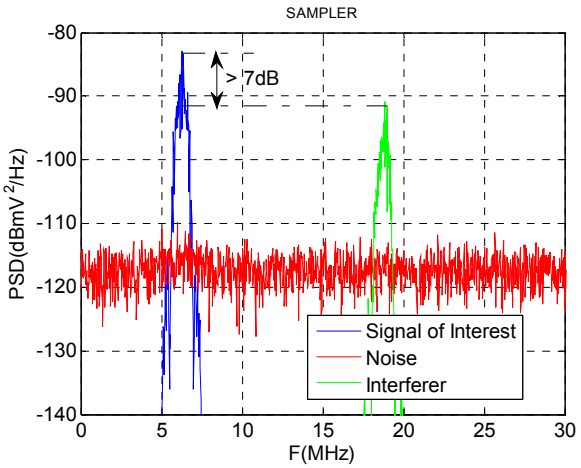


Figure 4-23 : The signal spectra after sampling

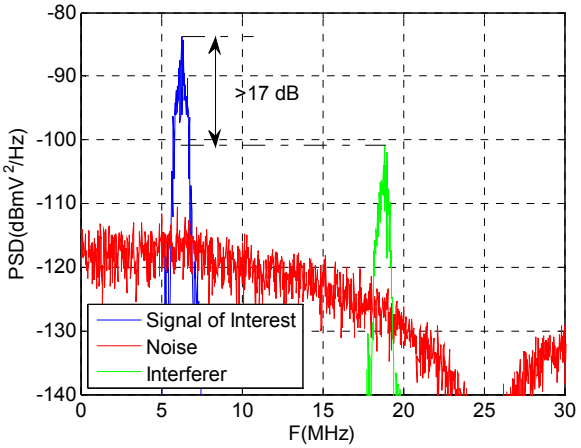


Figure 4-24 : The signal spectra after DT filtering

The initial interferer PSD is 27dB above the signal PSD and is 7dB below after the last CT filter . The missing 10dB rejection is therefore completed on the DT filter Figure 4-24, validating it for the application on the ULP RF standard. In Table 4-8 are summarized the resulting simulated SNR and SNDR for different test benches.

Standard	Test Bench	SNDR(dB)
Bluetooth Low Energy	Sensitivity	14.15
	Int @ Δf=24MHz	14.4
	Int @ Δf=50MHz	15.2
	Int @ Δf=75MHz	14.1
	IIP3	14.3
IEEE802.15.4	Sensitivity	3.7
	Int @ Δf=25MHz	6.9
	Int @ Δf=50MHz	6.9
	Int @ Δf=70MHz	6.9
	IIP3	6.4

Table 4-8 : Summary of the simulated SNDR for in presence of interferers

In conclusion the proposed IF voltage sampling relaxes the "gm" requirements on the sampler level, while the selective IF1 filter makes it still possible to relax the ADC dynamic range requirements. The application of a low IF2 with a selective IF1 filter allows implementing the down-conversion in single path, reducing significantly the number of blocks on the receiver. The possibility to split the in-band interferer rejection requirements into CT and DT filters enables to derive simplified configurations for both filtering techniques. The CT filter implements a second order elliptic filtering function while the DT filter is a simple 4th order Sinc filter and decimation by 4. Although it brings together the advantages of applying low IF2 and still relaxing the ADC constraints, the use of a high LO frequency on the mixer increases the constraints on the frequency synthesis blocks. Another risk on this architecture is that the architecture performance relies on a selective IF1 filter which is not yet implemented, and represents a technology challenge to control the required transfer in the perspective of implementation.

On the following, the novel proposed architecture targets to link the advantages of low-IF, relaxed ADC dynamic range also in combination with the use of low LO frequencies. This is possible applying high IF1 frequencies, where the IF1 filter can be implemented with classical BAW technology, which is more reliable and can be used on a demonstration of the DT receiver concept. In the next section, the architecture is presented in detail and dimensioned for the proposed applications. This architecture is the benchmark of the rest of the thesis, thus an advanced description and specification is provided.

5 New Architecture Proposition: high IF Bandpass sampling Combined with a Complex DT filtering to low-IF

5.1 Architectural Description

The previously presented architectures use various possibilities of BPS in order to down-convert and demodulate the RF signal. The various receiver blocks specifications for the BT-LE and IEEE802.15.4 have been defined through system level design method and simulation tool presented in CHAPTER 3. The results highlight the following drawbacks on the previous architectures:

- When high sampling frequencies or mixer LO are used, the frequency synthesis blocks represent the critical part of the receiver. The PLL / DLL output buffers present a large amount of the power consumption budget of a receiver, presented in the state of the art in CHAPTER 2. On the charge sampling side, low sampling frequencies are impractical. In this case, multiples stages on the DT filter and decimation lead to complicated switched capacitor blocks.
- When quadrature BPS is applied directly on RF, quadrature LO is needed. I / Q mismatches limit the signal SNDR or image rejection in the case of low-IF.
- When the zero-IF is applied, additional constraints in terms of power consumption appear in order to reduce 1/f noise. DC offset and second order distortion impacts the signal SNDR.
- Low-IF are required to achieve selectivity on the analog filtering for image rejection on the IF sampling architecture. High frequency LO is needed in this context.

Out of the presented trade-offs, the solution to avoid a given drawback result in creation of another. Therefore, it was proposed a novel architecture able to overcome the described drawbacks together, which are summarized in Table 4-9:

Drawback	Solution
High reference frequencies	High IF1: low f_{OL} and high under-sampling ratio: low fs
DC offset, IIP2, 1/f noise	Low IF3 architecture
Image filtering at high IF1	Complex DT filtering
Complex BPS I/Q mismatch	Complex TF through Hilbert transform on the DT filter with single sampling frequency

Table 4-9 : The BPS sampling architecture drawbacks and the proposed new architectures solutions

The proposed architecture is illustrated in Figure 4-25. Similar to the architecture of section 4, the architecture employs the use of an anti-aliasing CT filter at IF1. The LO on the mixer works at low frequencies, in the range of f_{OL}=400MHz - 480MHz (differently from section 4). The first IF1 is around IF1 ≈ 2GHz, with the anti-aliasing CT filter applied. From IF1, a high sub-sampling ratio is applied through voltage sampling. As defined in CHAPTER 2 - section 1,

the derived aliasing factor depends on the in-band/out-of-band noise ratio which is linked to the pre-sampling gain, in this case, the LNA and MIXER gains.

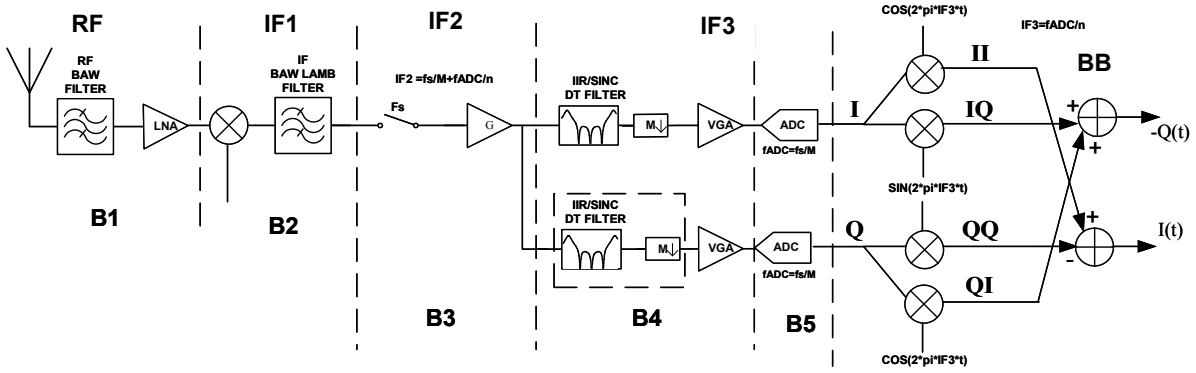


Figure 4-25 : High IF1 architecture, IF1 CT filter and BPS voltage sampling, complex DT filtering @ IF2

As presented in section 4, the interferer rejection constraints are split amongst the CT and DT filtering. The IF1 filter of section 4 is applied at relatively low IF1 in order to implement the image rejection and a low IF2 architecture. The main difference in the proposed architecture is that the CT filter does not need to be selective enough in order to make image rejection. Complex DT filter is applied for image rejection. The IF1 filter does not need to be narrowband, and considering the constant kt^2% over the frequency, high IF1 can be targeted. In consequence, the mixer LO frequency f_{OL} can be reduced. BAW, BAW-Lamb or SAW are possible technologies to implement such filter. A more in-depth analysis on the filtering function is presented in section 5.3.

As above-mentioned, the application of low *fs* simplifies the DT filter and decimation steps. During the BPS process, the signal is down-converted to a second IF2, where the center frequency of the complex DT filter is located, optimizing the DT filtering function. On the filter output, the signal is decimated and down-converted from IF2 to a low-IF IF3 which is chosen in order to avoid constraints such as 1/f noise and DC offset problems. The DT filter is applied in order to complete in-band interferer rejection and to implement image rejection on IF2 level. On the digital domain, the signal is down-converted to base band and demodulated using a modified weaver structure [22], by an ASIC or a FPGA. In this stage also, the base band channel filtering is completed and implemented at f_{ADC}. On the following section is presented the frequency plan which manages to match the position of the down-converted signals and the filters center frequencies. It will be observed that the ADC can present a variable f_{ADC} to demodulate several channels. The interface to the rest of the signal processing consists of a non-integer decimation block [7].

5.2 Frequency Plan

The first constraint regarding the frequency plan is the IF1 filter technology. The first hypothesis is that IF1 is fixed. We define the frequency plan starting from the ADC up to IF1. The ratios between the various frequencies presented in Figure 4-25 will be defined. First, the last IF, IF3, is defined as an integer ratio of f_{ADC}.

$$IF3 = f_{ADC} / n \quad (n \in Z^+) \tag{4-3}$$

The integer ratio is needed in order to ease the digital demodulation and down-conversion from IF3 to base band. As it was used on the architectures of section 2 and 4; n=4 is also applied in this case. A digital cosine at $f_{ADC}/4$ is simply the [1 0 -1 0] sequence, the sine is [0 1 0 -1].

The decimation process to f_{ADC} on the DT filter also implements the down-conversion, which is from the second IF2 to the third IF3:

$$IF2 = f_{ADC} + IF3 = f_{ADC}\left(1 + 1/n\right) \tag{4-4}$$

The decimation order on the DT filter M is set between fs and f_{ADC}. M is also the order to the DT filter. In terms of fs, equation (4-4) becomes:

$$f_{ADC} = fs / M \quad (M \in Z^+)$$

$$IF2 = fs \cdot \left(\frac{1}{M} + \frac{1}{M \cdot n}\right) \tag{4-5}$$

It was defined between the first IF1 and fs a high sub-sampling ratio. On the BPS process, the N^{th} harmonic of fs transposes the signal from IF1 to IF2:

$$IF2 = IF1 - N \cdot fs \tag{4-6}$$

$$IF1 = fs \cdot \left(N + \frac{1}{M} + \frac{1}{M \cdot n}\right) \tag{4-7}$$

Considering that IF1 is fixed (depending on the CT filter center frequency), the local oscillator down-converts each RF channel to IF1:

$$f_{OL} = f_{RF} - IF1 \tag{4-8}$$

In this configuration it appears that f_{OL} and fs are independent since IF1 is fixed. In order to avoid a very complicated frequency, a limited fractional ratio *K* (ex:3,5; 4; 4.5) is defined between fs and f_{OL}:

$$f_{OL} = K \cdot fs \tag{4-9}$$

We analyze the consequence of applying (4-9) on the frequency plan. We link IF1 to f_{RF} through the application of (4-9) on (4-7):

$$IF1 = f_{RF} \cdot \frac{1}{1 + \frac{KM}{NM + 1 + 1/n}} \tag{4-10}$$

In order to illustrate the multiple down-conversions and the chosen frequency plan, Figure 4-26 shows the demodulation of a signal at f_{RF}: a given channel inside the BW_{RF}. In this case if K, M, and n are fixed values, IF1 will vary in the same range of f_{RF}. We define two numerical applications on the frequency plan considering the BT-LE and the IEEE802.15.4 standards. The first considers a fixed IF1 and therefore fixed fs. M, K, N and n will be fixed values linked to implementation issues. The second considers that N and K vary. N is by definition and integer value in order to respect the frequency plan but K is the link between f_{OL} and fs in this case decided to be multiple of 0.5.

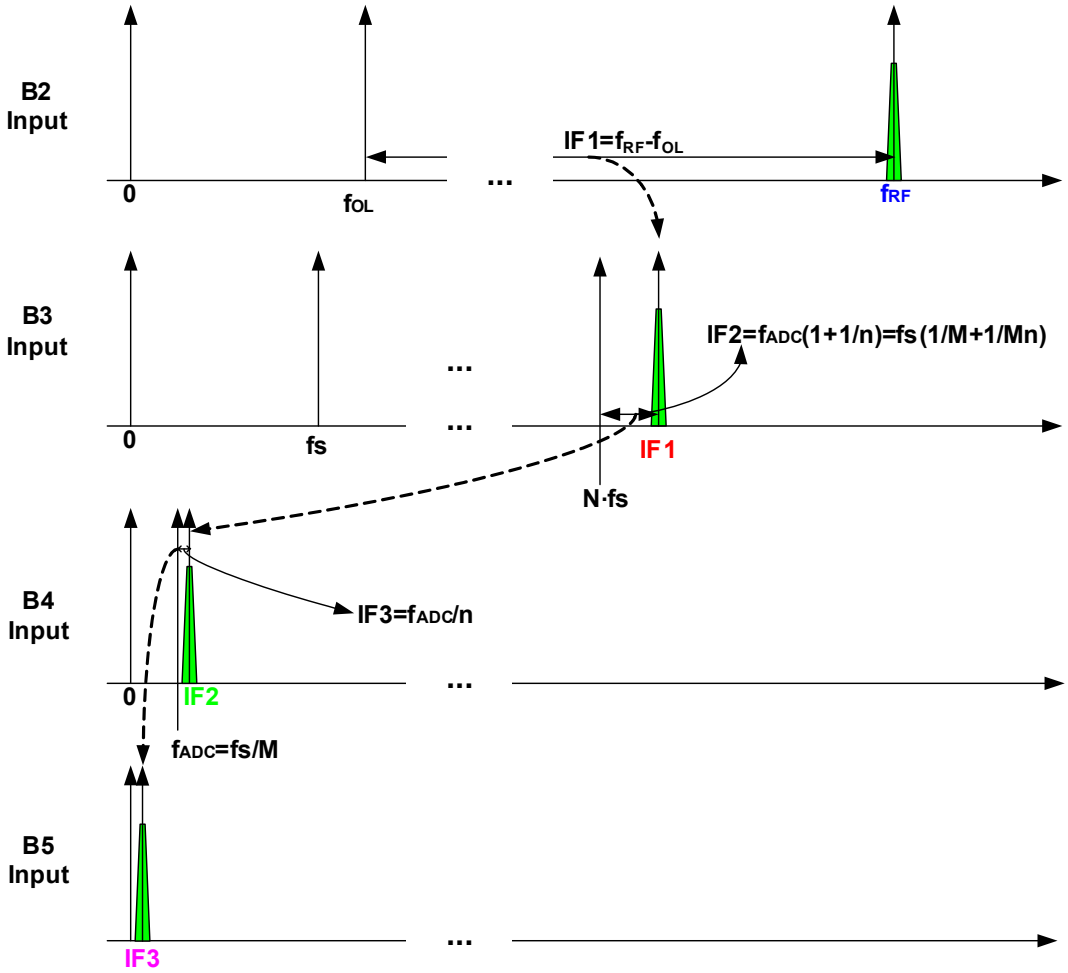


Figure 4-26 : The multiple down-conversions on the proposed architecture

5.2.1 Numerical application of the frequency plan with fixed IF1

In this numerical example, fs is independent from f_{OL} and a high IF1 is required. First hypothesis concerns the sampling frequency. At IF1 stages, signals which are potentially aliased at IF2 are located at (N-1)fs+IF2 and (N+1)fs+IF2. The filtering strategy considers that the IF1 CT filter does not completely reject the in-band interferers, which is then completed by the DT IF2 filter. This implies that during the sampling process the aliasing region must be placed outside the standard overall bandwidth (Figure 4-27). This aliasing interferer is an out-of-band interferer, where the RF front-end filter in addition to the CT filter implements the required rejection. For the ULP RF standards, BW_{RF}=80MHz.

As illustrated in Figure 4-27, in order to avoid in-band aliasing interferer, the following relations must be respected:

$$\begin{aligned}(N+1)fs + IF2 &> Nfs + IF2 + BW_{RF} \\ (N-1)fs + IF2 &< Nfs - (BW_{RF} - IF2)\end{aligned} \qquad fs > BW_{RF} \tag{4-11}$$

Considering f_{ADC} fixed and below 25MSPS [82] and (4-11), we conclude that the minimum decimation order is M=4 and so is the DT filter order. The sum of the CT IF1 and DT IF2 filters implements the in-band-interferer rejection.

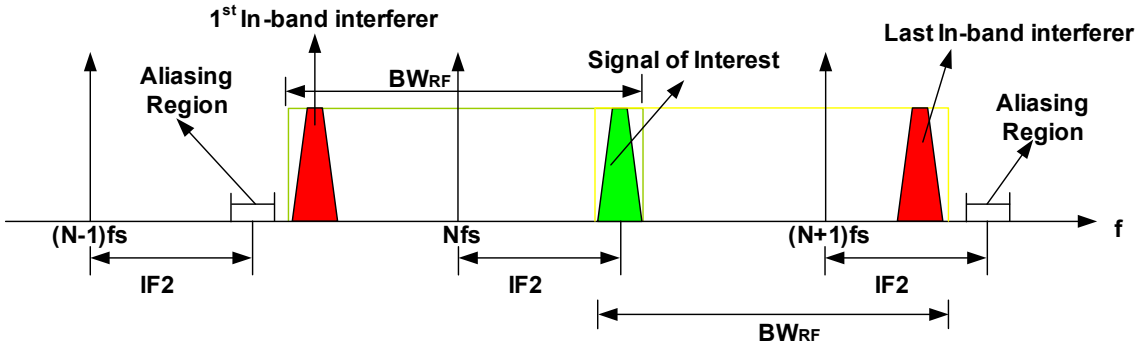


Figure 4-27 : The sampling frequency condition for non in-band interferer aliasing

The exact f_{ADC} is obtained considering that the channels for BT-LE are spaced every 1MHz. By choosing f_{ADC} a non-integer multiple of 1MHz, the aliasing region does not fall exactly in the region of possible interferers (Figure 4-28), relaxing aliasing interferer rejection. Choosing f_{ADC}=24.5MHz, with M=4, the sampling frequency becomes fs=98MHz and respects relation (4-11).

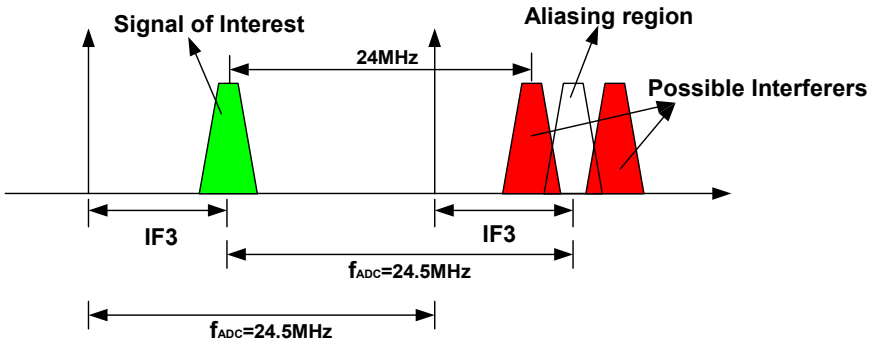


Figure 4-28 : The aliasing at the decimation and f_{ADC}

As presented in section 4, the low-IF at $f_{ADC}/4$ leads to a simpler implementation of the digital down-conversion to base band. Here, n=4 is defined as well. In order to have a low power configuration on the frequency synthesis stage, the LO is set as f_{OL}<500MHz. IF1 is therefore around 2GHz. Following (4-7) and considering IF1≈2GHz, we derive the value for N and for f_{OL}:

$$IF1 = 1990.6MHz \qquad for \qquad N = 20$$

The mixer f_{OL} varies with steps of 1MHz, from f_{OL_min}=409.375MHz to f_{OL_maxn}=489.375MHz in order to address the RF band f_{RF}=2.4GHz - 2.48GHz. The frequency plan is summarized in Table 4-10.

Frequency type	Value (MHz)
IF3	6.125
f_{ADC}	24.5
IF2	30.625
fs	98
IF1	1990.625
f_{OL}	409.375:1:489.375
f_{RF}	2400:1:2480

Table 4-10 : The proposed receiver frequency plan for fixed IF1

Whenever there are variations on the IF1 filter center frequency due to implementation process deviations, the frequency plan is recalculated for the new IF1. From frequency synthesis point-of–view, it implies a reconfigurable reference frequency for the LO and the sampling clock. In order to reduce the constraints on the frequency synthesis, a varying *IF1* is considered, where *K* is chosen from fixed values in such a way that f_{OL} and *fs* can be implemented in the same frequency synthesis block. This technique is explained on the following section.

5.2.2 Numerical application frequency plan with varying IF1: Illustration of the System Reconfigurability

In this application, the factor K which links f_{OL} to fs, is going to be fixed to defined values. As described in the previous section, IF1 is set around IF1≈2GHz in order to have f_{OL} below 500MHz. In the previous section, IF1 has been fixed and N=20 derived. In order to have the same filtering blocks on both numerical applications, n and M are kept the same as the previous example (n=M=4). This configuration allows to simplify the frequency synthesis by linking the LO to the sampling frequency by fixed values. We illustrate the fact the filtering functions are adapted to various frequency plans and can be adapted to variations on the CT filter parameters (variable IF1). We consider equation (4-10) in the case where K=4 is fixed. Figure 4-29 shows the application of (4-10) addressing the ISM band. Different modes of N are illustrated (from 15 to 22). Consider the case when IF1 is centered at 2.044GHz (black rectangle of Figure 4-29) the first RF channel is addressed with N=22 and IF1=2.035MHz as the RF channel changes, IF1 changes following the blue line. When two lines coincides in addressing the RF channel the mode is changed (N=21 in this case) and IF1 decreases again to the starting point (IF1=2.035MHz). In Figure 4-29, when the IF1 is centered at 1983MHz and the different modes are applied to cover the RF band, the variation between the lowest and highest IF1 is BW_{IF1}=22MHz.

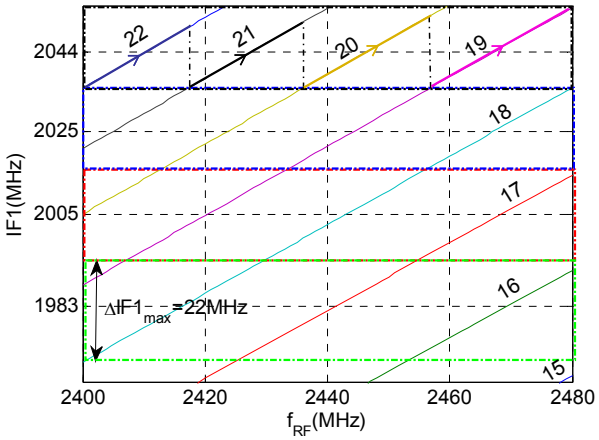


Figure 4-29 : *IF1* vs f_{RF} for K=4

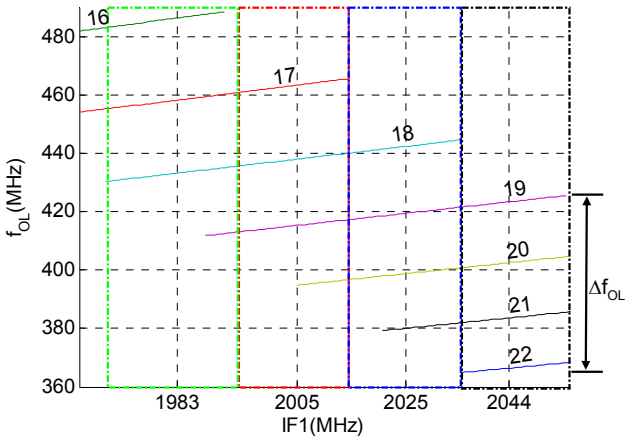


Figure 4-30 : f_{OL} vs *IF1*

Another interesting characteristic is that along the various operational modes, different center frequencies for IF1 can be addressed. In the case of Figure 4-29, the center IF1 can vary from 1983MHz to 2044MHz. The proposed frequency plan and the DT filtering functions allows for the receiver to address a wide range of IF1. The variation on the CT filter center frequency for example can be compensated by simply changing the operational modes. In Figure 4-30 is

illustrated the corresponding f_{OL} for each operational mode and RF channel. For example, if the IF1 region is represented by the black rectangle, then N=18 to N=22 and f_{OL} varies from 365MHz to 425MHz.

In cases where the IF1 CT filter does not present a bandwidth as large as the one presented on the numerical example of Figure 4-29, it is then interesting to decrease BW_{IF}. For that, the *K* factor can be non-integer. In the next example IF1 is set IF1≈2GHz and different modes of K can be combined with N. In Figure 4-31 is illustrated the variation of IF1 when K=4 or K=4.3 combined with different modes of N. Combining the different modes, BW_{IF1} reduces to 14MHz, which relaxes the CT IF1 filter specifications, while the same range for IF1 from 1983MHz to 2044MHz can still be covered. In this example the range of variation for IF1 is reduced to BW_{IF1}=14MHz which is illustrated in Figure 4-31 by the region between IF1=1978MHz to 1992MHz. In conclusion, the dynamic frequency plan is a solution to define a trade-off between the frequency synthesis complexity and the CT filter technology deviation. The DT filtering function follows the different sampling frequencies respecting still the specifications while the different operational modes link the LO to the sampling frequency. The possibility to address various central IF1 shows the reconfigurability feature for the architecture related to possible CT technology deviations.

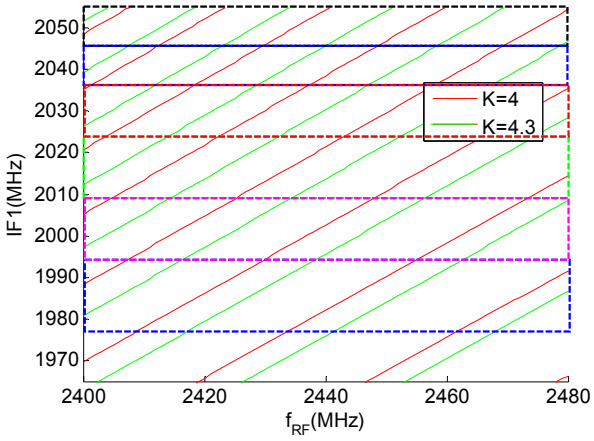


Figure 4-31 : *IF1* vs f_{RF} for K=4 and 4.3

5.3 The filtering techniques and the filtering masks

We remind the RF standards specifications and the system level design method in CHAPTER 3. Considering the required SNDR for both standards, Table 4-11 summarizes the interferers and image rejection required for the standards:

Parameter	IEEE802.15.4	BT-LE
In-Band Interferer rejection	36.5dB	44dB
Image rejection	not specified	26dB

Table 4-11 : The filtering specifications

In order to define the filtering masks, the frequency plan described in 5.2.1 is adopted. In this case, we applied a non-varying IF1. A deviation on the center IF1 is addressed by reconfigurable f_{OL} and fs in to respect relation (4-7). The filtering mask is set considering the required rejections and the position in the spectrum of the harmful interferers. From the resulting mask, the filtering techniques will be defined and discussed. On the mixing process, there is a first image signal IM_{RF} centered at f_{RF}-$2f_{OL}$ (Figure 4-32). From Table 4-10, we can infer that the first image frequency range is between 1502MHz to 1582MHz. The IM_{RF} rejection is implemented by the front-end filter, which from literature ([113]), presents out-of-band rejections >40dB, in our case, greatly superior to the required specifications. At the sampling stage (Figure 4-26), the distance between the N^{th} harmonic and IF1 sets IF2 and an image frequency IM_{IF1} is present at IF1-2·IF2 (Figure 4-33). From Table 4-10 IM_{IF1} is 60MHz away from IF1. This sets the first specification on the CT IF1 filter.

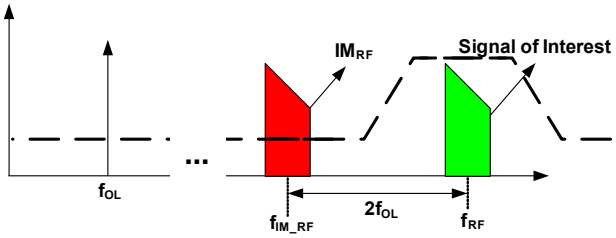


Figure 4-32 : The image signal on the RF level

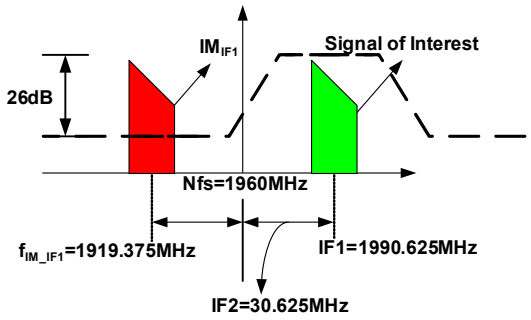


Figure 4-33 : The image signal on the IF1 level

At the decimation stage, the down-conversion from IF2 to IF3 sets a third image frequency region IM_{IF2} at IF2-2·IF3 (Figure 4-34). The negative side of the image signal folds on the IF3 band. One of the filtering requirements of the proposed DT complex IIR filter on the architecture illustrated in Figure 4-25 is the image filtering of IM_{IF2}. The required rejection of 26dB is obtained by a 4^{th} order FIR and 1^{st} order IIR complex filter (Figure 4-37). In-depth study on the DT filter theory, implementation and performance is presented in detail in CHAPTER 5.

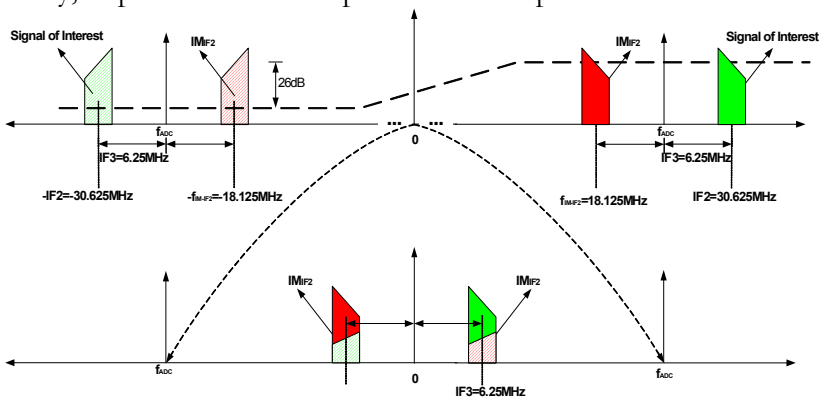


Figure 4-34 : The image signal on the IF2 level

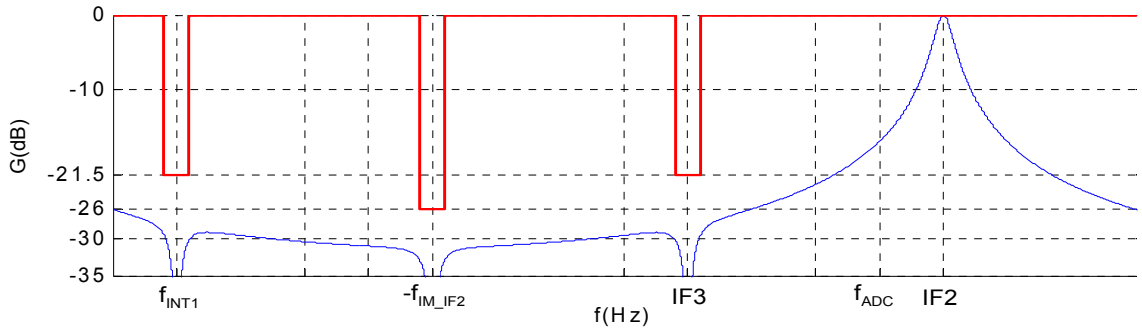


Figure 4-35 : The complex DT filter performance

As observed, the pass-band of the filter is centered at IF2 and there is a notch in the image frequency at -fim=-fs/4+fs/16 and image rejection of Δ_{im}>30dB is achieved. During the BPS process and on the decimation process, various in-band interferers fall inside the band of interest. The decimation process makes the spectrum periodic to the decimated frequency, therefore it can be seen as resampling the system. Considering the aliasing process presented in CHAPTER 2 and the sampling frequency with f_{ADC}, the possible aliasing interferers can be identified directly in the IF1 level (Figure 4-36).

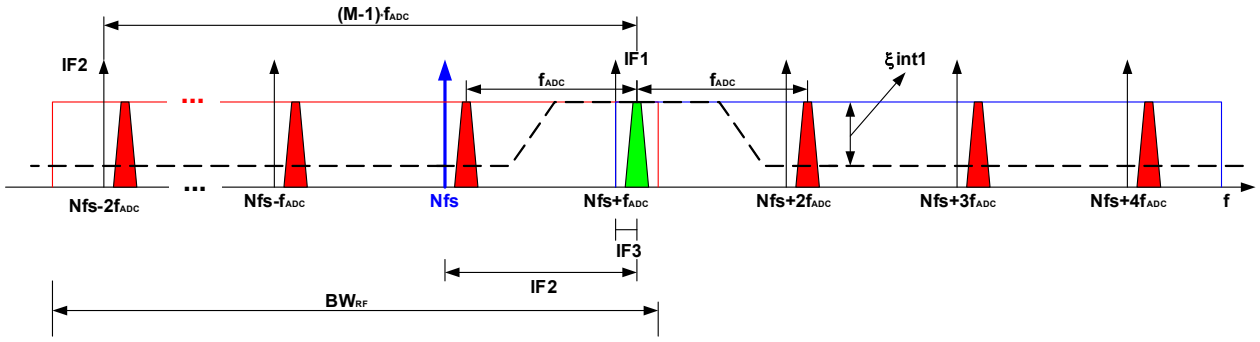


Figure 4-36 : The possible aliasing interferes analyzed on *IF1* level

As observed the aliasing interferers are at IF1 $+nf_{ADC}$ (n=-2,-1, ...,+4). Although the aliasing occurs only after decimation, a part of the interferer rejection Δint1 can be implemented in a first stage (Figure 4-36). From the architecture in section 4, the need to split the filtering constraints between CT and DT filtering has been observed in order to achieve the required specifications. In the IF1 stage the required 44dB from Table 4-11 does not need to be completely achieved.

In order to understand how the interferer rejection is split into these two techniques, the performance of the complex DT filter is analyzed. From Figure 4-35 we observe notches at $f_{ADC}/4$ and -3 $f_{ADC}/4$. Finally, after decimation, the interferers at $f_{ADC}/4$ and -3 $f_{ADC}/4$ are aliased into $f_{ADC}/4$=IF3. The interferer rejection Δint=44dB is obtained by the sum of the rejections indicated on Figure 4-36 and the one obtained at the notches of the DT filter, which are Δint >27.5dB. Considering 6dB margin for the DT filter performance, the required aliasing interferer rejection for the DT is Δint =21.5dB (indicated on the filtering mask of Figure 4-35). The remaining rejection specifications of 22.5dB is the filtering mask for the CT IF1 filter at IF1 $+nf_{ADC}$ (n=-2,-1, ...,+4).

The filtering mask for the CT IF1 filter consists on considering the image rejection of Figure 4-34, the interferer rejection on Figure 4-36 and a third constraint for the wideband noise anti-aliasing specifications. The aliasing factor definition is presented in CHAPTER 3, and from an allowed aliasing factor and the input noise bandwidth before sampling, the wide anti-aliasing rejection is defined through (CHAPTER 3-part 3 equation). Considering the frequencies presented in Table 4-10, the filtering mask is summarized in Figure 4-37.

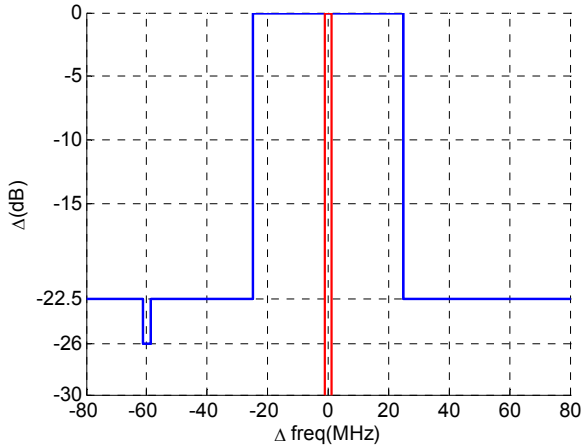


Figure 4-37 : The specified filtering mask for the CT analog *IF1* filter (Figure 4-25)

5.3.1 Continuous Time analog IF1 filter implementation

The implementation of the CT IF1 illustrated in Figure 4-25 was the subject of a study carried out during an internship in the LAIR laboratory which I had oriented and followed. From the developed mask, it had analyzed the possibility of implementing such filtering function through the use of resonators, more precisely the BAW Lamb technology [73]. The particular interest for this type of filter is the possibility to implement on the same chip also the FBAR mode RF front-end filter. Another great advantage is the possibility to implement high characteristic impedance, which reduces the driving currents for this block, reducing transconductance constraints. The filtering function is based on the resonator structures and the electrical coupling between these resonators. Filtering networks such as ladder and lattice [114] had been studied during the internship and the basic electrical model adopted for the piezoelectric resonator structure is a *Modified Butterworth-Van Dyke* (MBVD) model [115]. The filter design is detailed in APPENDIX C . The method is based on respecting a given prototype filter following a certain filtering function. In order to respect the filtering mask, a 2nd order elliptic prototype filter has been applied, which corresponds to a second order lattice filter. The simulated filter, through MVBD model, the reference prototype filter and the required mask are illustrated below:

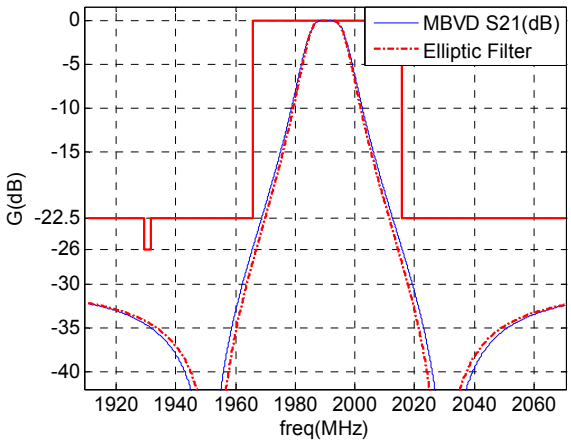


Figure 4-38 : The analog CT filter performance for the prototype and simulated MBVD S21

The filter selectivity depends on the filter notches, and the last one defines the filters out-of-band rejection as well. For the second order elliptic filter, the selectivity is attained for an out-of-band rejection of 31dB. This out-of-band rejection will be further used to calculate the aliasing factor due to the BPS process. The proposed filter implementation type is able to respect the filtering masks with a simple filtering network while applying innovative BAW Lamb technology, which presents the previously mentioned advantages. In the next section, we define the block specifications for the architecture Figure 4-25. To do so, the architecture is split in active blocks, the SNR and SNDR degradations are set and the blocks specifications are calculated through the use of the system level design methodology of CHAPTER 3.

5.4 System Level Design and Validation

First, the architecture illustrated in Figure 4-25 is divided into active blocks. Initial hypothesis are defined in order to set the correct constraints distribution. First, at the ADC level, of which power budget is expected to be under P_{ADC}=1mW. The applied ADC sampling frequency and resolution are f_{ADC}=24.5MHz and neff=5bits, which are in agreement with the low power ADC state of the art presented in CHAPTER 2. Considering a flat quantization noise ADC, the equivalent noise figure referred to 50Ω is $NF_{50\Omega}$=75dB (equation 30 CHAPTER 3).

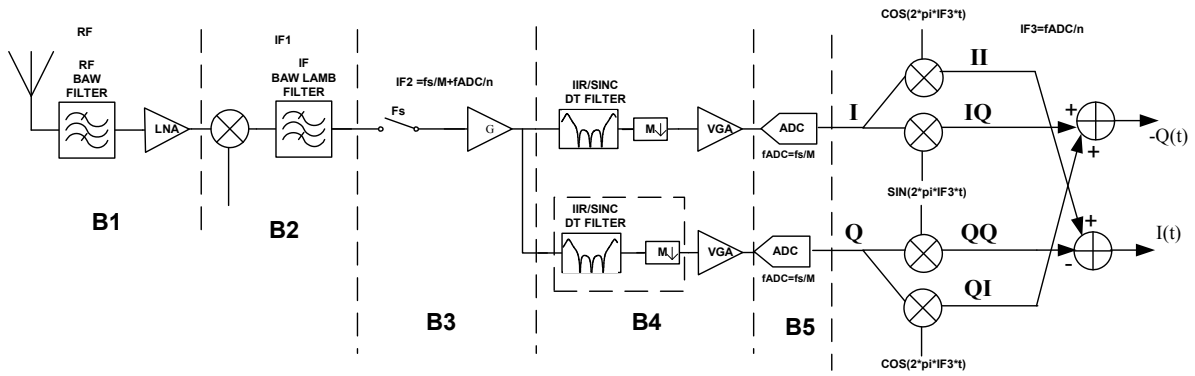


Figure 4-39 : The definition of the proposed architecture active blocks

Second hypothesis is the sample-and-hold noise model for a given capacitance value. As presented in CHAPTER 2, there is a trade-off between the gain bandwidth product for the

sampler and the noise generated by the sampling capacitor. Considering a bandwidth of IF1≈2GHz and a limit on the transconductance gain of 10mS leads to the maximum sampling capacitor of Cs=800fF. With the sample-and-hold noise defined in equation 15 of CHAPTER 2 and the sampling frequency of fs=98MHz, the equivalent sampler noise figure referred to 50Ω is set to $NF_{S/H}$=27.2dB. Further in CHAPTER 5 we calculate the equivalent NF for the sampler and the DT filter. The NF of B4 is derived and the required gain of B3 is set in order to respect each standard specifications.

5.4.1 The SNR and SNDR degradation distributions and Blocks specifications

The idea of defining a distribution of constraints between blocks was first introduced in [98]. It is stated that local improvement in a block performance has more impact on the overall performance when the constraints are equally distributed than otherwise. Although this statement is correct, it does not lead to realistic implementation of the blocks, mainly in terms of low power configuration on the front-end blocks (the frequency of operation is not considered). In [116], the system design method of CHAPTER 3 is presented. Not only several distributions on the SNR degradation can be applied, but also a new parameter called aliasing factor is introduced in order to consider the design of BPS architectures. Comparing to constraints distribution in low power receivers, and the state of the art on the low power basic blocks of CHAPTER 2, the first adopted SNR degradation distribution for the proposed architecture is $1/X^2$.

On the following, the blocks performances are compared with expected performances for the sampler and ADC blocks and the front-end presented on the state of the art of CHAPTER 2, and the next iteration occurs, which also relies on design experience. The state of the art is low power oriented, which validates the dimensioning in terms of power consumption. As it was defined for the total gain in the section 2, the strongest interferer test bench P_{int_max}, is set then the maximum ADC input dynamic range. The possible adjacent rejection is obtained from Figure 4-38. Table 4-12 summarizes the receiver parameters able to define the total gain:

	Parameter	Value
Front-end Conditions	Z_{ant}	50 Ω
	V_{p_p}	1V
	P_{ADC_max}	21dBmV²
BlueTooth Low Energy	P_{int_max}	-23dBmV²
	Δ_{adj}	4dB
	Gv_{max}	48dB
IEEE802.15.4	P_{int_max}	-35dBmV²
	Δ_{adj}	4dB
	G_{max}	60dB

Table 4-12 : Receiver parameters defining the total gain

The required SNR/SNDR considers the theoretical BER vs SNR relations defined in CHAPTER 3 for the ULP RF standards. The total SNR and SNDR degradation are calculated

through equation 10 of CHAPTER 3. Table 4-13 summarizes the SNR degradation and gain per block of Figure 4-39 for the ULP RF standards. In order to apply the indicated sampling capacitance on both configurations, IEEE802.15.4 requires more gain prior to sampling (precisely on the mixer stage, B2). More gain applied earlier implies that the blocks IIP3 from the sampler to the ADC undergo the need for more linearity.

The RF front-end filter used as reference in the architecture (Figure 4-39) is designed through BAW FBAR technology. It was developed for the EURIMUS project EPADIMD EM91 (European Platform for Advanced active Implantable Devices) in the LETI laboratory and the measurement results are used in the simulation chain. The filter presents losses of 2.8dB. Since B1 considers both LNA and RF filter, the LNA required performance is $G_{LNA}=G_{B1}+G_{RF\_F}$ and $NF_{LNA}=N_{B1}-N_{RF\_F}$. On B2, the mixer and the IF1 CT filter are considered. If implemented in BAW Lamb technology, the filter resonators present a quality factor up to Q=1000 [117]. While applying the filtering network presented in APPENDIX C and the given quality factor, the calculated losses are around 1.7dB. Considering a margin to define the IF1 filter losses, G_{IF1_F}=-3dB. As for LNA depends on the B1 specs, the Mixer requirements consider the B2 specifications, $G_{MIXER}=G_{B2}+G_{IF1\_F}$, $NF_{MIXER}=N_{B2}-N_{IF1\_F}$. Comparing the blocks performances for B1 to B3 with the state of the art from CHAPTER 2 we understand that the derived specifications lead to very power consuming configurations for both LNA and Mixers.

Standard	Parameter	B1	B2	B3	B4	B5	TOTAL
BlueTooth Low Energy	Gv (dB)	11	0	10	27	0	48
	SNR_{deg}(dB)	11.7	3.9	5.8	1.9	5.7	29
	γ	1	2	1.7	1	1	-
	NF 50Ω(dB)	11.7	19.3	29.8	38.8	75.7	-
	$SNDR_{deg}$(dB)	13.4	5.8	6.3	3.3	6.2	35
	IIP3 50Ω(dBmW)	-26	-18	-22.6	-14.5	-5.7	-
IEEE802.15.4	Gv (dB)	11	6	10	33	0	60
	SNR_{deg}(dB)	11.2	4.1	3.6	0.9	1.7	21.5
	γ	1	2	1.7	1	1	-
	NF 50Ω(dB)	11.2	19.9	30.1	38.6	75.7	-
	$SNDR_{deg}$(dB)	12.2	4.7	3.5	1.3	2.8	24.5
	IIP3 50Ω(dBmW)	-25.5	-15.3	-11.5	-2.5	-3.7	-

Table 4-13 : Summary of the block specifications for the architecture in Figure 4-25

The system blocks specifications are set for the required SNDR thanks to the system design method. To further understand the filtering functions, verify the aliasing factor in a simulation environment, and validate the performances of Table 4-13 on the given test benches, the proposed architecture is modeled through the system level simulation tool developed in MATLAB (chapter3).

5.4.2 System Level Simulation: Fine Tuning of Specifications and Architectural Validation

Some critical aspects of BPS architectures are verified thanks to the system level simulation. The first is the simulated aliasing factor. As presented in CHAPTER 2 the aliasing factor γ is dependent on the following parameters:

- The input noise PSD and BW
- The sampling frequency
- The anti-aliasing filter out-of-band rejection and losses.

The filter losses are considered as wideband thermal noise sources, which define a noise floor on the filter output. The input noise PSD depends on the previous blocks gain and NF. From equation 11 of chapter 2 the aliasing factor of γ=1.7 is calculated for a noise bandwidth of BW_{Neff}=4GHz. The equivalent BW_{Neff} considers a first order low-pass filter for the sampling block at a cut-off frequency of fc=2.5GHz. The considered in-band/out-of-band noise PSD ratio was Δ_{noise}=16.8dB. On the simulation tool, the frequency response of Figure 4-38 is applied. Figure 4-42 illustrates the resulting PSD on the IF1 CT filter output. The simulated aliasing factor is γ_{SIM}=1.72, which validates the expect aliasing factor from Table 4-13.

Another critical aspect is the validation of the frequency plan and filtering functions. To do so, several techniques are applied on the filter models. The RF front-end filter is modeled using the S parameters file from measurement results (Figure 4-40) of the RF filter developed in the LETI laboratory. The CT IF1 filter is obtained through the MBVD model for the filter of Figure 4-38 and the calculation of the S parameters considering impedance matching on input and output. The details on the components values on the MBVD model are given in APPENDIX C . On the simulation tool, the calculations are implemented in frequency domain in order to improve the simulation speed. The calculation coefficient for the proposed filter of Figure 4-39 is derived in CHAPTER 5.

In order to verify the required interferer rejection specifications of Figure 4-38 and Figure 4-35, a test bench for BT-LE containing an interferer @ Δf=25MHz from the signal of interest is applied. We remind from 5.2.1 that the aliasing region is at Δf=24.5MHz but the interferers are 1MHz from each other, therefore Δf=25MHz is chosen for this test bench. Figure 4-41 and Figure 4-42 show the spectra before and after IF filtering, and in Figure 4-43 and Figure 4-44 we observe the signal spectra before and after DT decimation filter.

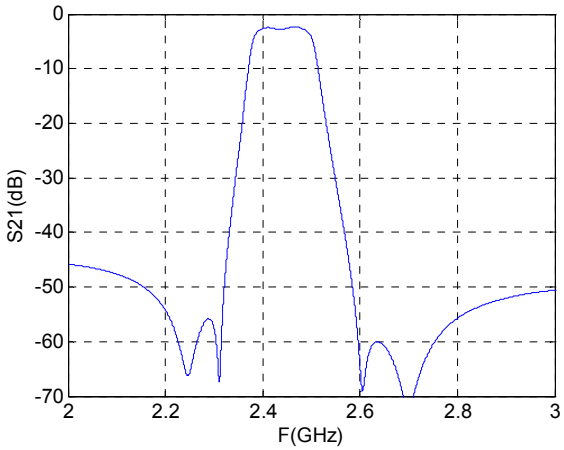


Figure 4-40 : RF filter S21

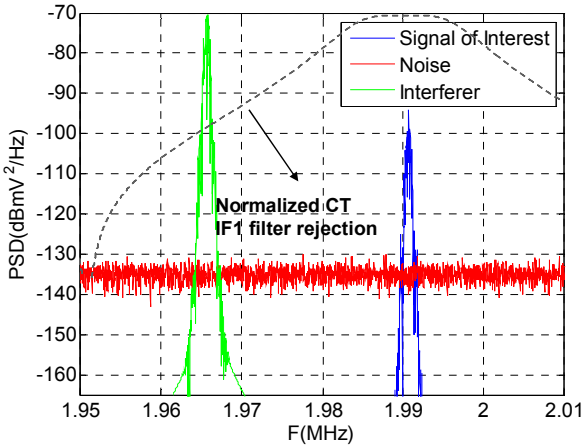


Figure 4-41 : The signal spectra on the IF1 filter input

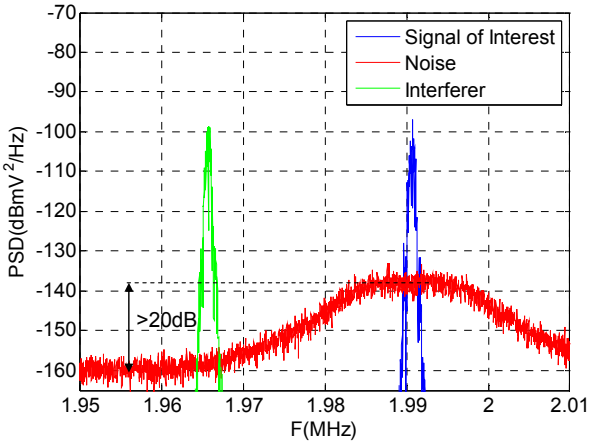


Figure 4-42 : The signal spectra on the IF1 filter output

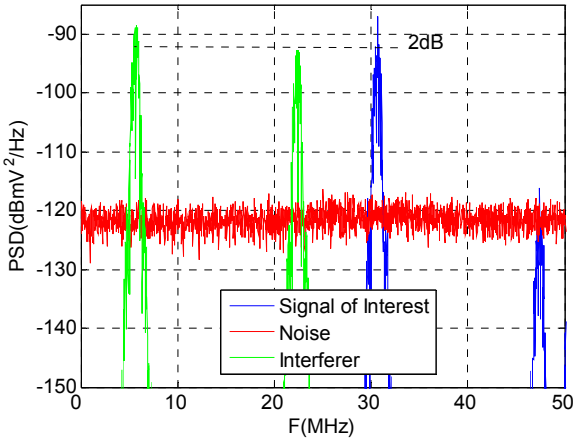


Figure 4-43 : The signal spectra on the DT filter input

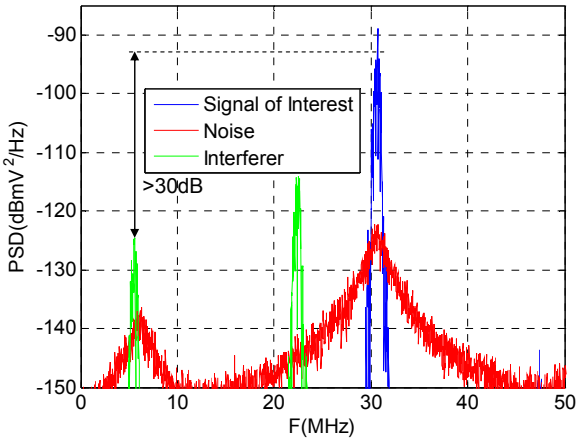


Figure 4-44 : The signal spectra on the DT filter output

The simulated spectra from Figure 4-41 to Figure 4-44 show that the interferer rejection are respected with considerable margin (Δ>60dB), Δ=32dB for the DT filter (see Figure 4-33), and Δ=28dB from the IF1 DT filter (see Figure 4-38), observed for a distance of @ Δf=25MHz.

The same analysis is carried out in the case of the image frequency @ IF1-2·IF3. The image test bench is defined in table 6 of CHAPTER 3. The main characteristic of this complex

DT filter is the filter notch placed at the image frequency position. Figure 4-45 and Figure 4-46 show the complex spectra (I+jQ) before and after DT filter for the image interferer test bench.

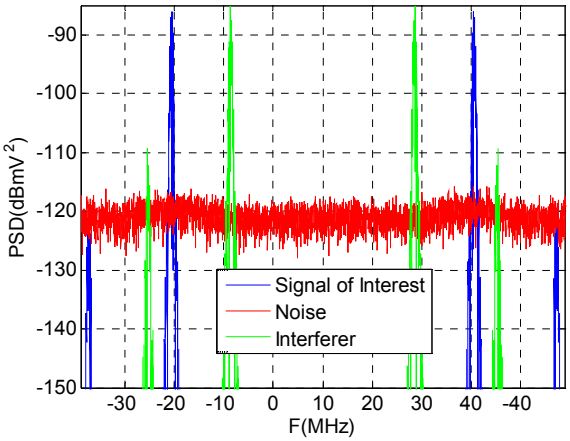


Figure 4-45 : The signal spectra on the DT filter input for the image rejection TB

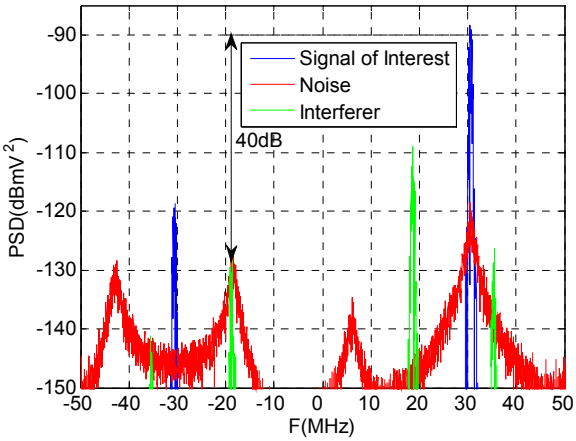


Figure 4-46 : The signal spectra on the DT filter output for the image rejection TB

From Figure 4-39 we observe that block B4 contains a filtering and amplification stage. Further in CHAPTER 5, the filtering+VGA block will be detailed, implementing a first FIR stage and the IIR stage including the VGA the IIR feedback loop. Therefore, the selective filtering of Figure 4-35 is implemented at the VGA output, which means that the ADC is the only block of which IIP3 is relaxed thanks to the more selective transfer function of the DT filter. The VGA IIP3 is therefore close to the one defined in Table 4-13. The system level method considers active macro blocks Bn. On the simulation tool, each component Bn_m is simulated separately, and the blocks on Figure 4-39 are separated as follows:

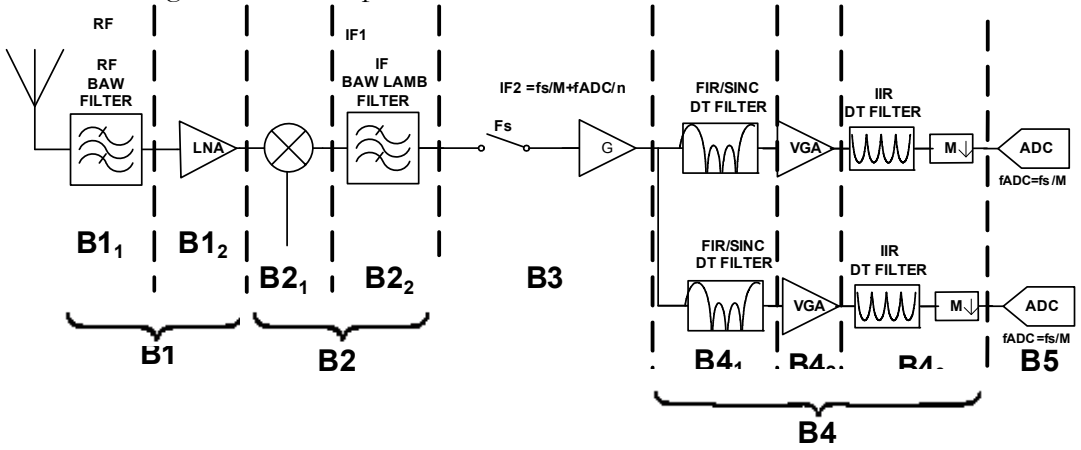


Figure 4-47 : The definition of the blocks of the proposed architecture for the simulation tool

For the sensitivity test bench, Figure 4-48 and Figure 4-49 illustrate the SNR vs block and the required SNR at the ADC output on. A set of test benches with aliasing interferers and image signal have been defined in order to validate the proposed architecture. Based on Figure 4-36, the aliasing interferers can be defined on the f_{RF} frequencies at $f_{CH}+nf_{ADC}$ (n=-2,-2,…,+4); from the standard specifications of CHAPTER 1, interferers are also defined to be spaced at least at multiples of 1MHz (the case for BT-LE). The applied image frequency test bench is as defined for IM_{IF2} (Figure 4-34) where the image rejection is tested for the DT IF2 filter. The SNDR after the ADC is evaluated for each test bench. Table 4-14 summarizes the resulting SNDR for each test bench.

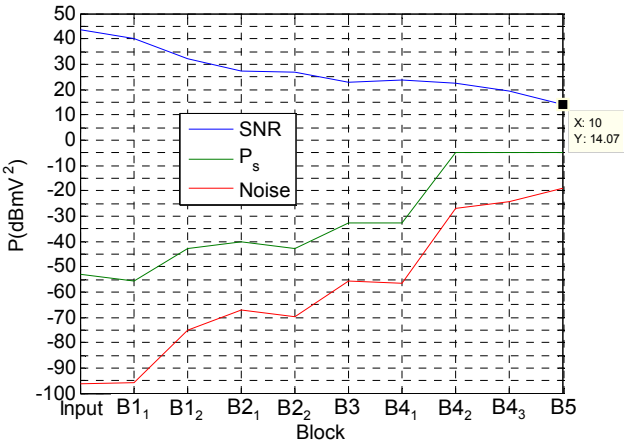


Figure 4-48 : Simulated SNR per block, BT-LE

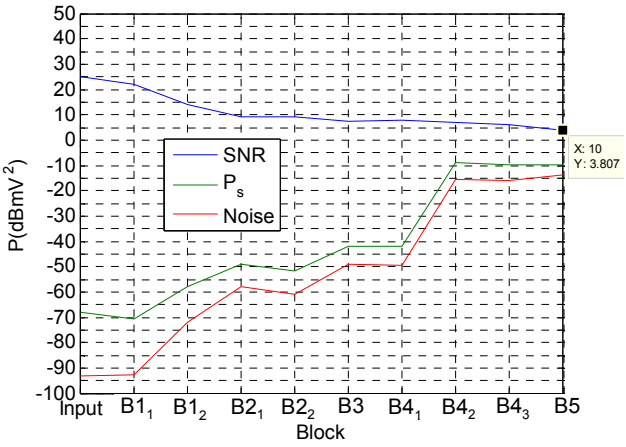


Figure 4-49 : Simulated SNR per block, IEEE802.15.4

Standard	Test Bench	SNDR(dB)
BlueTooth Low Energy	Image @ Δf=12MHz	16.8
	Int @ Δf=25MHz	15.6
	Int @ Δf=50MHz	16.6
	Int @ Δf=75MHz	16.4
IEEE802.15.4	Image @ Δf=10MHz	5.8
	Int @ Δf=25MHz	6.1
	Int @ Δf=50MHz	7.1
	Int @ Δf=75MHz	6.7

Table 4-14 : Summary of the simulated SNDR for in presence of interferers

For the IIP3 test bench the interferers' amplitude undergoes the nominal gain minus the rejection from Figure 4-35, for the calculation on Table 4-13. In the case of IEEE802.15.4 there is no precise test bench to test IIP3. The receiver linearity can be inferred considering the desired signal in the presence of two interferers, adjacent and alternate channels [102], as detailed in CHAPTER 3. Figure 4-50 and Figure 4-51 illustrate the IIP3 test bench for BT-LE. The increase of the non-linear distortion over the noise floor is verified on the VGA and ADC blocks. In the IIP3 test bench, the desired signal is 6dB over the sensitivity, where the noise floor is set.

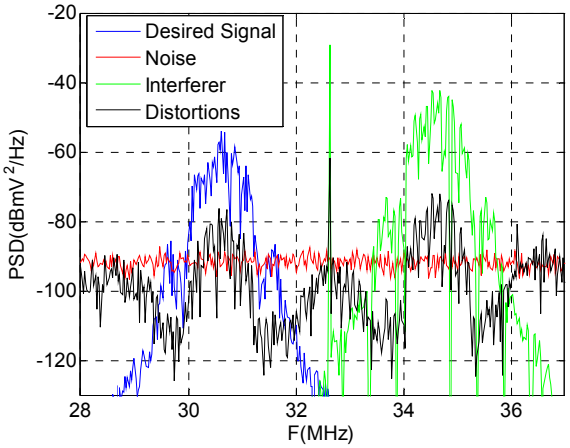


Figure 4-50 : Signal spectra on the VGA output for the IIP3 test bench of BT-LE

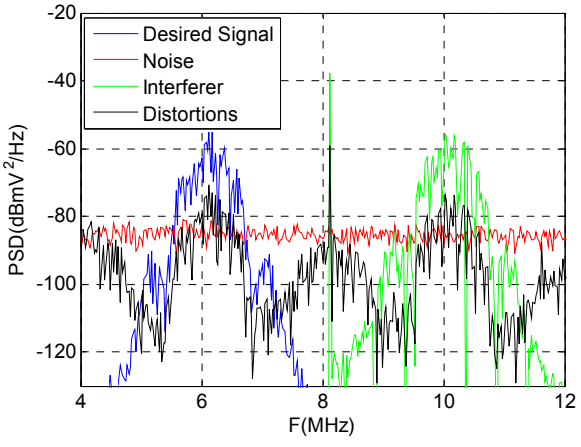


Figure 4-51 : Signal spectra on the ADC output for the IIP3 test bench of BT-LE

Figure 4-52 and Figure 4-53 illustrate the SNDR vs block for the IIP3 test bench for BT-LE and IEEE802.15.4. Notice that it is possible to visualize the impact of the various contributions on the SNDR and that the required SNDR is respected.

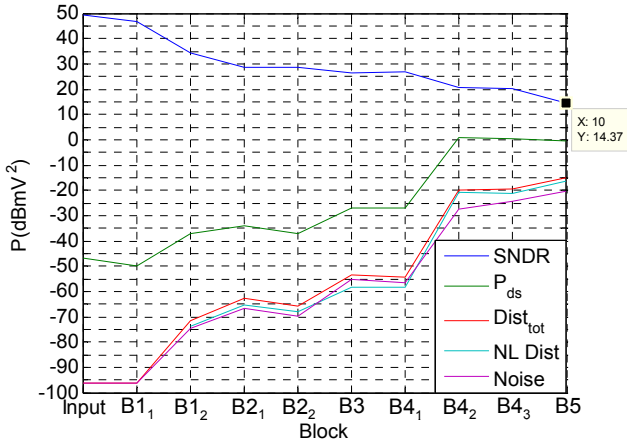


Figure 4-52 : Simulated SNDR per block for the IIP3 test bench, BT-LE

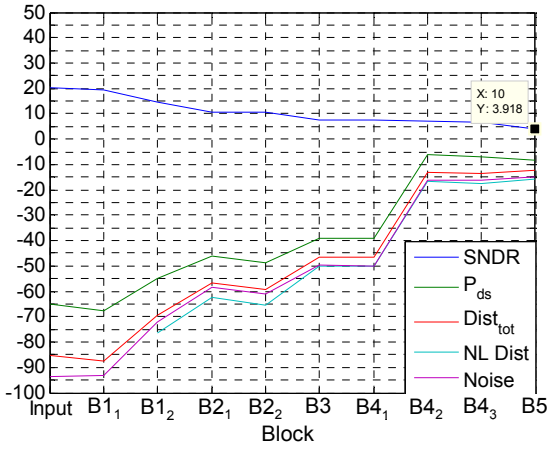


Figure 4-53 Simulated SNDR per block for the IIP3 test bench, IEEE802.15.4

The fine definition of the IIP3 specifications is therefore obtained through iterative system simulation, providing with the new specifications summarized in the Table 4-15:

Standard	Parameter	$B1_1$	$B1_2$	$B2_1$	$B2_2$	B3	$B4_1$	$B4_2$	$B4_3$	B5
Bluetooth Low Energy	IIP3 50Ω(dBmW)	-	-23.5	-16.5	-	-20.5	-	-14.2	-	-4.5
IEEE802.15.4	IIP3 50Ω(dBmW)	-	-25.5	-15	-	-11.2	-	-1.5	-	-2.2

Table 4-15 : Summary of the block IIP3 definition through the system simulation tool

As observed, the most impacted blocks are on the receiver back-end, where the high input power makes the last blocks saturate. n conclusion, we validate the specifications from Table 4-13 through the simulation environment. On the aliasing test benches (image and in band interferer), the margins obtained in this chapter will be used on the block implementation analysis of CHAPTER 5 for the DT complex filter, mostly on Monte Carlo analysis on the deviation from the nominal frequency response. And finally on the IIP3 test bench, the blocks saturation and gain blocking in addition to the application of modulated signals, allows tuning the blocks IIP3.

As a result of the system level design through the application of more precise modeling, the system specification is defined with fewer margins where considerable amount of power consumption can be saved. The overall block specifications present balance between different blocks constraints. The blocks specifications are in agreement with low power configurations on the front-end implementation when compared to the state of the art of CHAPTER 2.

5.5 Conclusions on the Proposed Architecture

In this section, a novel architecture exploiting the use of high sub-sampling ratios has been presented in order to reduce the frequency synthesizer constraints. The use of DT signal

processing allows the receiver to adapt over IF change due to manufacturing/ageing/temperature deviations. The use of complex filtering allows to avoid Zero-IF architecture and to decimate the system down to frequencies where low power ADCs can be used. The DT filtering network is simplified by the use of IIR structure and the application of pre-filtering on the IF1 level. The share of the interferer rejection specifications between the CT IF1 filter and the DT filter allows defining and optimizing a solution which simplifies filtering techniques. The overall specifications are attained through the proposed system level design methodology, including the constraints distribution and the system simulation tool. The results are summarized in Figure 4-54. The blocks specifications are in agreement with low power configurations.

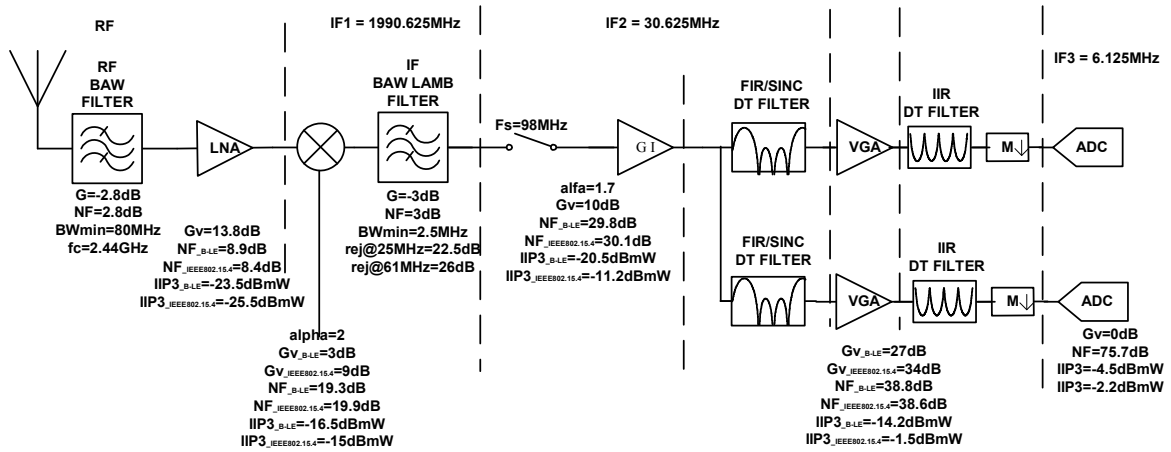


Figure 4-54 : The proposed architecture and the required performances

The overall results show the interest of applying BPS architecture in order to achieve ULP and digital-like / agile receivers. The architecture has a frequency plan which makes it possible to address various IF1 frequencies in order to compensate technology variations of the CT IF1 filter. This reconfigurability does not impact the block specifications which are still valuable for the ULP RF standards. This is only possible by adopting a DT domain signal processing, which transfer functions follow the sampling frequency. The DT time processing of the proposed architecture is based on charge sharing and relative capacitor size, which we verify in CHAPTER 5 to be very robust to technology deviations, and therefore, more adapted to sub-micron technologies.

6 Conclusion

In this chapter various BPS sampling architectures have been defined for the ULP RF standards. In order to do so, a novel system design method and simulation tool has been developed to consider the particularities of BPS (mainly on the DT signal processing and on the wide band spectrum aliasing). While various techniques on the BPS process have been analyzed, the system level analysis leads to the proposed architecture step by step. It integrates most of the advantages found in the three previous solutions on both agility and low power consumption.

The proposed architecture aims to significantly reduce the receiver DT filter complexity while applying in-band interferer and image rejection. The choice of a CT IF1 filter around IF1=2GHz is based on the fact that, at this frequency, many filter implementations can be found

in literature, which guarantees its feasibility. Another interest of a high-IF is the reduction of the frequency to be synthesized with no particular constraints on the other blocks, considering the state of the art of CHAPTER 2. The dynamic frequency plan allows compensating deviations on the CT IF filter while addressing several standards minimizing the difference on the block performances.

To further evaluate the interest of the proposed architecture, two major points have to be verified: the DT filter feasibility and performances regarding front-end implementation imperfections and the frequency synthesis specifications, mainly phase noise and power consumption ones. In the next chapter we present the theory on the DT filtering. Through analytical development, behavioral modeling and simulation through VHDL-AMS language, we evaluate the impact of real block implementation imperfections on the proposed DT filter performances. On the last chapter, numerical developments evaluate the distortion caused by sampling jitter in BPS process. The applied methodology is presented and illustrated on the BPS context to derive the phase noise are derived for the proposed architecture. A comparison with the state of the art CHAPTER 2 allows evaluating the impact on the power consumption for the BPS process and the proposed architecture.

APPENDIX C THE IF1 CONTINUOUS TIME FILTER DESIGN

In order to implement the CT filters presented in the architecture of Figure 4-17 and Figure 4-25, a filter synthesis method based on [118] has been done. The application of the method in the study of the proposed architecture and BAW Lamb technology for IF filtering had been the subject of an internship which I supervised.

Lamb wave resonators [72] consist in a piezoelectric layer sandwiched between two thin electrodes. The resonance frequency is defined by the lateral propagation of acoustic waves (Figure 4-55). Lateral propagation poses no technological limit to the resonating wavelength. Therefore, the *LWR* can resonate at frequencies below 800MHz, contrarily to the thickness limit in vertical-wave propagation resonators. Lower center frequencies lead to narrower band filters, of particular interest for channel selection applications.

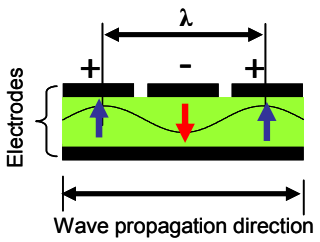


Figure 4-55 : LWR layers and function mode

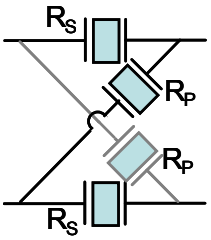


Figure 4-56 Lattice Network

The aimed filtering network is a lattice filter (Figure 4-56). This differential network is composed of series resonators Rs and crossed resonators Rp, and its transfer function is given by:

$$H(f)=\frac{Z_{Rs}(f)-Z_{Rp}(f)}{Z_{Rs}(f)+Z_{Rp}(f)} \qquad (4\text{-}12)$$

The distance between the resonance and anti-resonance frequencies of a resonator is proportional to a technological parameter called coupling factor kt^2 [118]. The filter pass-band is obtained by matching the resonance frequency of *Rs* with the anti-resonance frequency of *Rp*. The filter bandwidth BW_{LWR} depends on kt^2 and the center frequency. Transmission zeros are obtained when the series and crossed resonators present the same impedance (Figure 4-57) and they can be adjusted by modifying the ratio between the series and parallel resonator capacitances γ=C0s/C0p.

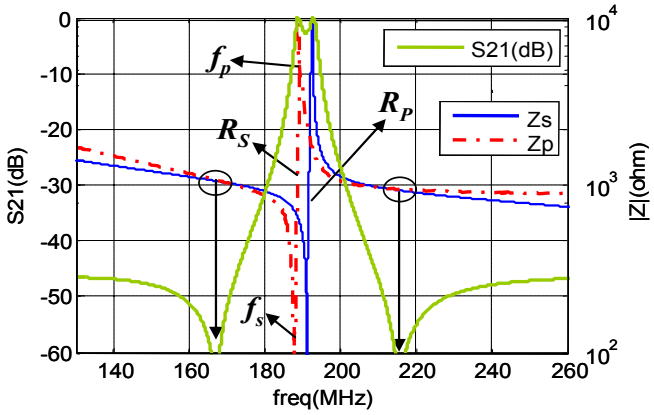


Figure 4-57 Lattice filter response and Z_{RS} and Z_{RP}

Figure 4-58 summarizes the employed algorithm based on [118]:

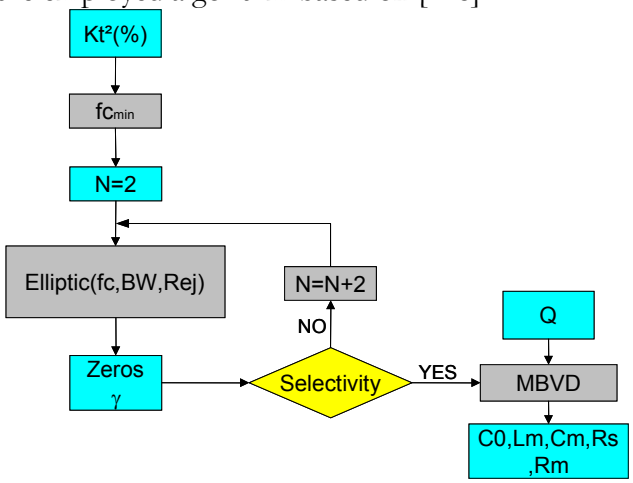


Figure 4-58 The filter synthesis method

First is set the coupling coefficient which is a technological dependent parameter. While choosing a required BW_{LWR}, a minimum filter center frequency is fixed. This is the case when selective filter is required in low IF1. In the case when a high IF1 is set, the center frequency and kt^2 are predefined and the resulting BW_{LWR} is fixed. On the other hand, fewer constraints on the filter selectivity are imposed in the case of high IF1.

The state of the art for the technology presents a coupling factor kt^2 between 0.6 and 1.6% [72]. The required BW_{ch}=2.45MHz for IEEE802.15.4 sets a minimum center frequency for the *LWR* filter of fc=250MHz when adopted kt^2=1%. In order to simplify the frequency plan on section 4 the IF1 center frequency for the proposed architecture in Figure 4-15 is fc=306.25MHz, the details are on section 4.2. In the case of high IF1, kt^2=1% @ IF1=1990.6MHz gives a BW_{LWR}(-3dB)=14MHz. The basic structure of Figure 4-56 represents a second order elliptic filter, which is used as prototype filter for the synthesis (Figure 4-58). First, one filter stage is considered, therefore a second order elliptic, then giving the required rejection, BW and center frequencies, the MATLAB function elliptic shows where the transmission zeros will be placed. The capacitance ratio γ is calculated from the distance between the transmission zeros and the fc.

In an elliptic filter, the further the transmission zeros, the better the out-of-band rejection and the worse the selectivity. The resulting frequency response is analyzed in terms of the required selectivity; if it is OK the components values of the MBVD [115] for each resonator are calculated. In both applications the second order elliptic is sufficient to respect the specifications. From the MBVD parameters, the filter designers can set the resonator dimensions and layout. The model is illustrated in Figure 4-59.

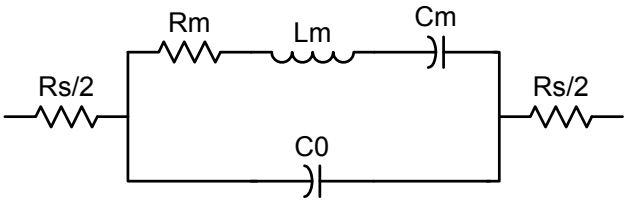


Figure 4-59 : The MBVD model

The static capacitor C0 is linked to the resonators surface and thickness and the resonators geometry. If only the top electrode is used using the basic resonator structure of Figure 4-55, lower capacitor can be achieved compared to a classical *BAW*. It is possible therefore to design filters presenting higher characteristic impedances [118]. Since in *IF* filtering there is no need to match to a low impedance like an antenna, higher impedances allow higher *Gain Bandwidth* products for a given power consumption budget. Lm and Cm, in addition to C0, set the series and parallel resonance frequencies (*fs* and *fp* of Figure 4-57). From the technology quality factor, losses on the resonator are calculated and the resistive components Rm and Rs are linked to mechanical and electrical losses, respectively.

In order to achieve the highest possible characteristic impedance, we remind the lowest static capacitance C0 related in the state of the art [72]. In [72], the characteristic impedance of *Zeq* of Zeq=1KΩ was attained for a center frequency of fc=233MHz, which means a minimum capacitance of $C0$=680fF.

Considering the reference technology and the lowest implement capacitance reported in [72], @ kt^2=1%, and Qs=900 and Qp=1000 from [117], TABLE summarizes the MBVD parameters for the filter of section 4 (fc=306.25MHz) and for the filter of section 5 (fc=1990.625MHz):

Figure 4-17			Figure 4-25		
Resonator	Parameter	Value	Resonator	Parameter	Value
Rs	Rs	9.9Ω	Rs	Rs	1.3Ω
	Rm	85Ω		Rm	11.88Ω
	Cm	707fF		Cm	7.27fF
	Lm	40μH		Lm	890nH
	C0	707fF		C0	717fF
Rp	Rs	9.5Ω	Rp	Rs	1.4Ω
	Rm	81 Ω		Rm	11.08Ω

	Cm	678fF		Cm	6.72fF
	Lm	38 μH		Lm	960nH
	C0	678fF		C0	672fF

Table 4-16 : MBVD parameters for the CT IF1 filters of Figure 4-17 and Figure 4-25

The MBVD parameters are therefore used to generate the Z and ABCD matrix for the lattice cellule. From the ABCD parameters it possible to evaluate the cascade of multiple stages, i.e., increasing the filter order by adding stages. The equivalent ABCD matrix is passed to S parameters for a given source and charge impedances. The resulting S parameters are used for the CT IF1 model applied on the system level simulation tool.

Chapter 5 : Implementation of the Complex IIR Filter

1 Introduction

In this chapter is discussed the implementation of the IIR complex filter, which appears in the proposed architecture of CHAPTER 4. At first, the basics on discrete time filtering are presented. The filter design starts from the most basic DT filter configuration: a Sinc FIR filter. On the following, the IIR filter basics aspects are presented. The structure presented is passed from FIR to IIR. After, the Hilbert transform is presented. This is used as a technique to shift in frequency the response of the filter to pass from symmetric real filter to a non-symmetric complex filter. The filter coefficients are therefore defined for the proposed filter in CHAPTER 4. Examples of analog implementation of a discrete time filter are presented theoretical explanation: FIR, IIR, FIR+IIR, complex IIR. The filtering network is based on charge sharing of switched capacitors. The filter schematics and the clock tree are presented. The capacitor values are calculated to perform the required *Transfer Function* (TF). For the IIR feedback loop, an *Operational Transconductance Amplifier* (OTA) is applied. Through the application of this network, the filter bandwidth and gain are reconfigurable by changing the capacitor pairs on the OTA feedback.

From the presented analog implementation of the filter, we analyze the block imperfections and their impact on the filter TF. The filter capacitor are implemented by combining multiples of a unit capacitance, causing an impact on the TF since a finite resolution is set on the filter coefficients. A unit capacitance is chosen considering this impact. On the following, a Monte Carlo study is carried out in order to validate the filter robustness to capacitor mismatch. Another aspect which is analyzed is the impact of the non-constant *Group Delay* (GD) of IIR filter on the signal *Error Vector Magnitude* (EVM). The level of distortion is compared to the allowed SNDR for the sampler and filter blocks introduced in CHAPTER 4. Noise is evaluated analytically and is compared to block implementation transient noise simulation for the FIR stage.

Further in the block implementation analysis, a behavioral model in *Very High Speed Integrated Circuits* (VHSIC) *Hardware Description Language* (VHDL) *Analog and Mixed Signal* (AMS), VHDL-AMS is developed for the filter. The parasitic capacitances impact on the filter TF is shown through this model. The non-linear behavior of the switches resistances is also analyzed through a parametrical VHDL-AMS simulation. A clock tree generation is developed in VHDL where the main issue is to avoid clock overlapping between rise and fall edges. The OTA is specified in terms of biasing, transconductance and output impedance focusing on the very low power configurations.

2 General principles of the IIR complex filter

2.1 Basic concept of a Discrete Time filter

In CHAPTER 2 the process of BPS has been introduced. The input signal, which has continuous amplitude and continuous time references, is first sampled in time and quantized in amplitude. Therefore we can define the sampling as an intermediate process before quantization in order to pass from the analog domain to the digital domain on the ADC.

Whenever the sampled signal enters in a process capable of memorizing the samples, the output of the system can be dependent of N values of the input of the system. In a linear system, the TF is defined by its impulse response [7]. We consider the impulse response h[n], decomposed in N branches:

$$h_k[n] = \begin{cases} h[n+k] & n = multiple\ of\ N \\ 0, & otherwise \end{cases} \quad (5\text{-}1)$$

The impulse response reconstruction is done by the following relation:

$$h[n] = \sum_{k=0}^{N-1} h_k[n-k] \quad (5\text{-}2)$$

On the following, we will discuss some techniques to compose DT filters by defining h_k. There are different techniques to implement a discrete time filtering [119, 120]. Classically it is implemented in digital domain where the blocks to implement the *Multiply-Accumulate* (MAc) operations are *Digital Signal Processors* (DSP), *Field Programmable Gate Array* (FPGA) and *Application-Specific Integrated Circuits* (ASIC). The choice depends on the level of reconfigurability and power consumption required by the application [119]. In our case, a reconfigurable ASIC based on the DT filtering is targeted since the application is limited to filtering and the focus is on low power consumption.

2.2 The Finite Impulse Response (FIR) filter

The simplest DT filtering network is known as the FIR filter. The output of an N^{th} order FIR filter is the sum of the N last inputs averaged by N coefficients b_n (Figure 5-1). Its discrete time TF is given by:

$$H(z) = \boldsymbol{Z}\{h[n]\} = \sum_{n=1}^{N} b_n z^{-n} \quad (5\text{-}3)$$

From the Discrete Fourier Transform, it is possible to find the poles and zeros of the discrete time TF and from the bilinear transform ([7]) we derive the frequency response for H(z). We are interest to analyze the TF of the 4^{th} order FIR, since it is the first component of the proposed filter.

$$H(z) = b_1 + b_2 z^{-1} + b_3 z^{-2} + b_4 z^{-3} \quad (5\text{-}4)$$

When b_n=1/4 for n=[1, 2, 3, 4], the filter frequency response is illustrated in (Figure 5-2)

The function is a sinus cardinal filter which notches are at n·fs/4 (n=[1, 2, 3, 4]) the order of the filter. This is the simplest DT filter also known by moving average filter. Used as decimation anti-aliasing filter, the filter notches are place at the decimation frequency.

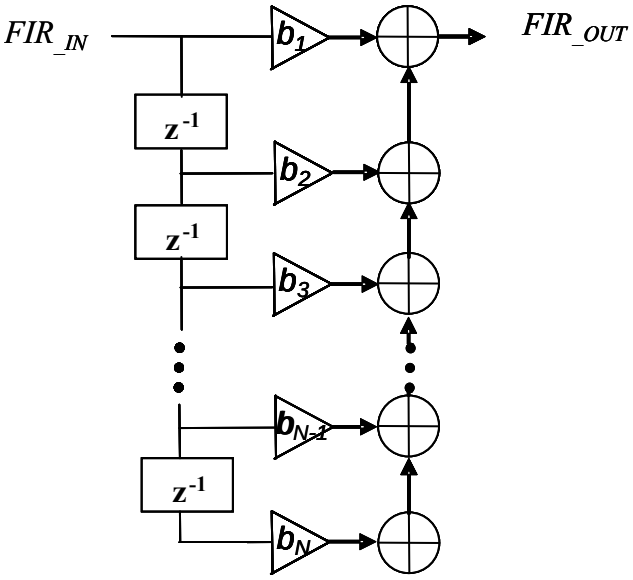


Figure 5-1 : Structure of a FIR filter

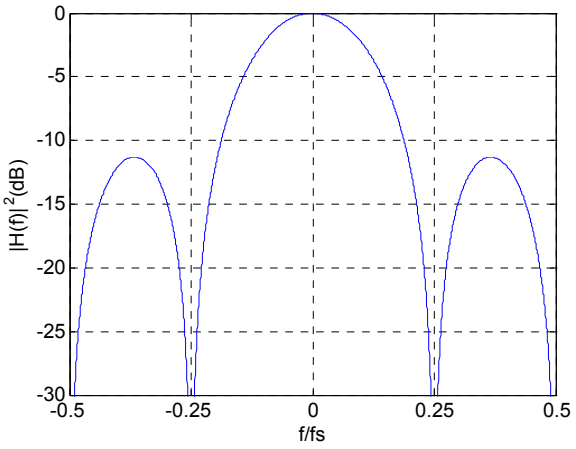


Figure 5-2 : |H(f)|(dB) for the FIR filter

2.2.1 Analog Implementation of the FIR filter

On the analog side, it is possible to implement the DT filtering, with the use of switched-capacitor blocks [2, 14, 17, 18]. The principle of the analog DT filtering is based on the capacitor charge sharing and charge transfer (in the case of an OTA), which implements the MAC operation. The Basic S/H+DT filter to implement the TF of (5-4) is given as follows:

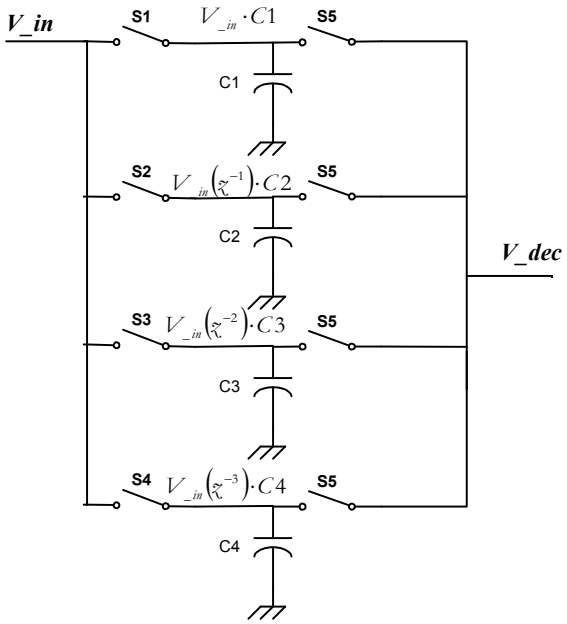


Figure 5-3 : Basic analog FIR Block Diagram

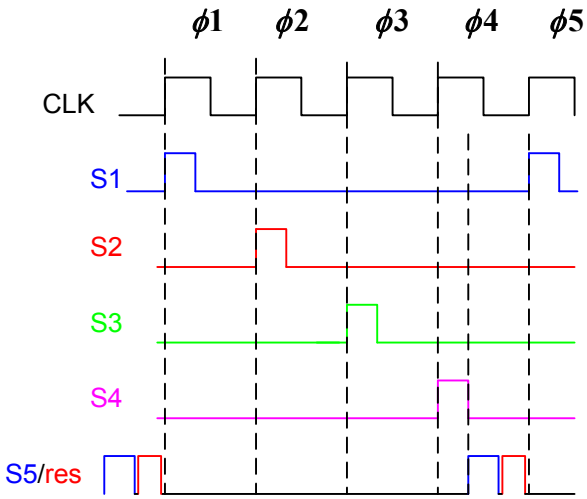


Figure 5-4 : Clock strategy for the FIR stage

In Figure 5-3, the capacitors C1 to C4 store the charges C1·V_in (z^{-0}) to C4·V_in (z^{-3}). The delay cells are actually the distance in time between the samples, i.e. 1/fs. After four samples

the stored values are charge-shared among the filter capacitors, this implement and weighted averaging operation, in other words, the MAC operation. All the capacitors are reset before the next cycle of samples. The critical time constant on the system is the reset. A duty cycle < 50% is applied on Sn (n=1…5) (Figure 5-4). One sample is given at the output every four samples of the input. The decimation by four is therefore intrinsic to the network, since it is not possible to keep the original charges from C1 to C4 after charge sharing. The order of the decimation is the same than the order of the filter unless we apply active blocks on the capacitors output in order to average the input without discharging C1 to C4. With equal capacitors the coefficients of (5-4) are generated. Since the network is completely passive, the gain is ideally "1" (but less than "1" due to charge losses). The TF is defined as follows:

$$H(z) = \frac{1}{\sum C_i}\left(C1 + C2 \cdot \left(z^{-1}\right) + C3 \cdot \left(z^{-2}\right) + C4 \cdot \left(z^{-3}\right)\right) \tag{5-5}$$

We derive the filter coefficients from the capacitor values:

$$b_n = \frac{Cn}{\sum_n Cn} \tag{5-6}$$

2.3 The Infinite Impulse Response (IIR) filter

Differently from the FIR filters, the IIR filter is not composed only by the combination of the last *P* input samples, but also of the last *Q* filter output samples. Compared to the FIR filter, the IIR presents better selectivity for the same filter order. For our application it provides channel selection which was not possible while using the FIR structure. The filter block diagram becomes:

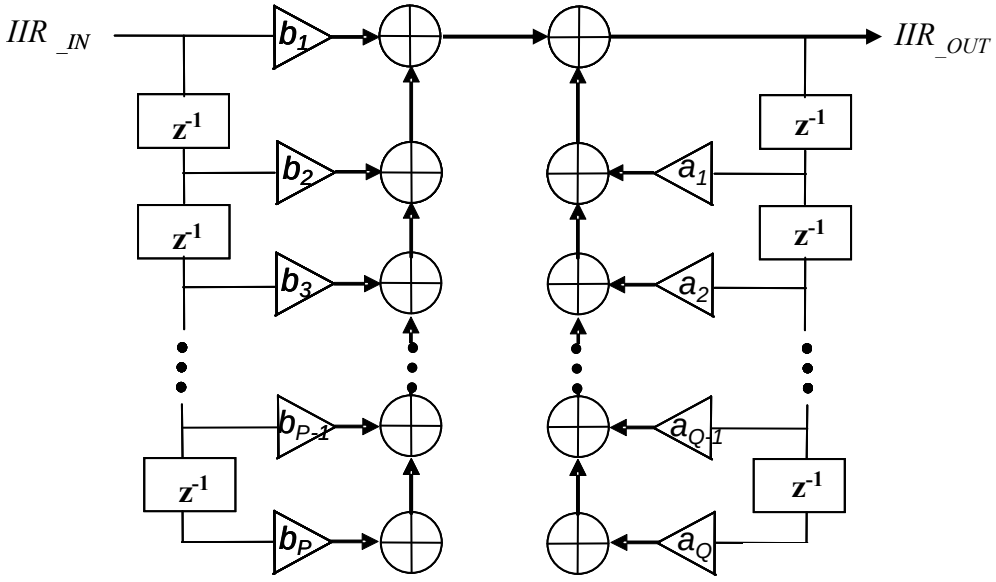


Figure 5-5 : Structure of a IIR filter

The discrete time TF is:

$$H(z)=\frac{\sum_{k=1}^{P} b_k z^{-k}}{\sum_{l=1}^{Q} a_l z^{-l}} \tag{5-7}$$

The denominator on (5-7) shows that the poles of H(z) can be different from zero (contrarily of the FIR structure). Therefore, the IIR can be unstable given the coefficient values. We analyze the following IIR filter which contains a single pole:

$$H(z)=\frac{\sum_{n=1}^{N} b_n z^{-n}}{1-\beta z^{-N+1}} \tag{5-8}$$

A system is stable if a bounded input sequence produces a bounded output sequence (BIBO) ([7]). For that the *Radius of Convergence* (ROC) of the system must include the unit circle. For (5-8) the ROC is defined for $\beta<|z|$, ([7] chap. 3.2); the system will be stable if $0<\beta<1$. We 4th order FIR is therefore added to the IIR network:

$$H(z)=\frac{b_1+b_2\cdot z^{-1}+b_3\cdot z^{2}+b_4\cdot z^{-3}}{1-\beta\cdot z^{-4}} \tag{5-9}$$

b_n =1 n=[1, 2, 3, 4]. The filter frequency response is given by:

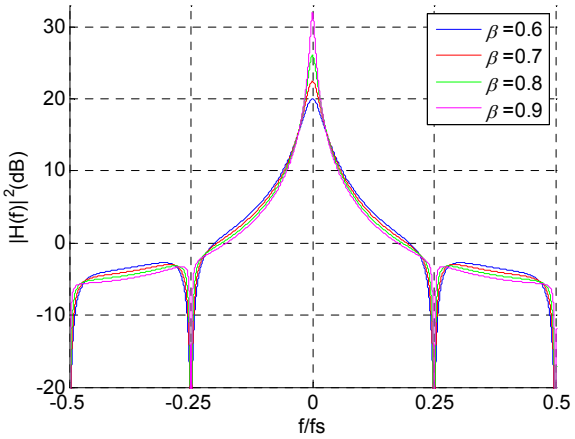


Figure 5-6 : Gain vs f/fs for the FIR filter

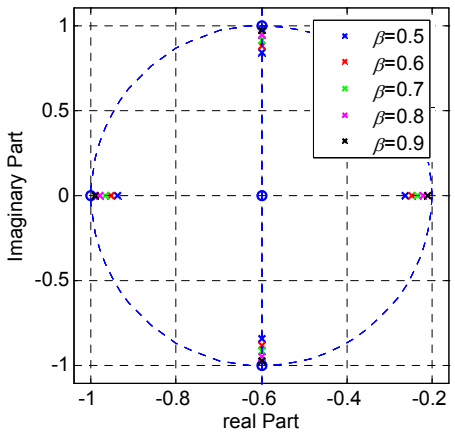


Figure 5-7 : ROC for the different IIR configurations

It is observed that when β gets close to 1, the filter gain increases and concentrates on the pole, therefore, it becomes more selective. We will further analyze the distortion on the filtered signal caused by such narrow band.

2.3.1 Analog implementation of the IIR filter - Application of an OTA

In order to implement an IIR filter, the output charge will be summed with a certain amount of the last output charge (given by β). In order to sum the charges without reducing the voltage level, it is important to have an active network implementing the feedback loop. A known structure able to implement such feedback is the inverting integrator ([121]-Part V):

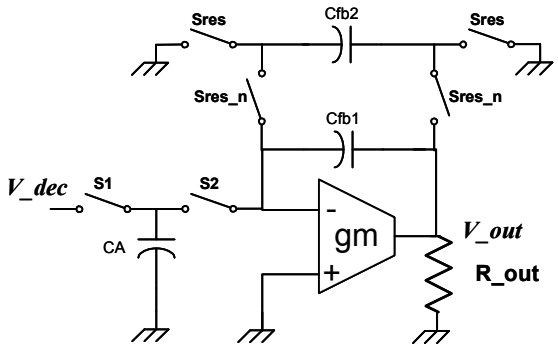


Figure 5-8 : Structure of the inverting integrator

As a first step, S1 is closed and the CA capacitor is charged, then, when S2 closes the charge on CA is transferred on Cfb1+Cfb2, which are discharged on an instant t=t0. We analyze the equation of charge conservation:

$$V_{dec}(n)\cdot CA + 0\cdot(Cfb1+Cfb2) = -V_{out}(n)\cdot(Cfb1+Cfb2)$$

$$\frac{V_{out}(n)}{V_{dec}(n)} = -\frac{CA}{(Cfb1+Cfb2)} \tag{5-10}$$

Now, consider that the initial charge on Cfb1 and Cfb2 is different from zero. Just before the charge is transferred, Cfb2 is reset and reconnected to Cfb1, which means that the initial value of $V_{out}(n)$ on the charge transfer is a ratio Cfb1/(Cfb1+ Cfb2) of the last output value:

$$V_{out}(n)\cdot Cfb1 = V'_{out}(n)\cdot(Cfb1+Cfb2)$$

$$V'_{out}(n) = V_{out}(n)\cdot\frac{Cfb1}{(Cfb1+Cfb2)}$$

Applying the charge conservation in this case:

$$V_{dec}(n+1)\cdot CA + V_{out}(n)\cdot\frac{Cfb1}{(Cfb1+Cfb2)}\cdot(Cfb1+Cfb2) = -V_{out}(n+1)\cdot(Cfb1+Cfb2)$$

$$V_{out}(n+1) = V_{out}(n)\cdot\frac{Cfb1}{Cfb1+Cfb2} - \frac{C1}{C2}V_{dec}(n+1) \tag{5-11}$$

The discrete time TF is therefore:

$$H(z) = \frac{V_{out}(z)}{V_{dec}(z)} = -\frac{CA}{Cfb1+Cfb2}\cdot\frac{1}{1-\beta\cdot z^{-1}} \tag{5-12}$$

$$\beta = \frac{Cfb1}{Cfb1+Cfb2}$$

With such configuration the feedback coefficient presented in Figure 5-6 is controlled by Cfb1 and Cfb2 and the closed loop gain on DC is defined by CA/((Cfb1+ Cfb2)(1-β)). This represents two degrees of reconfigurability on the architectural level since the BW and the gain of the filter network can be set with multiple configurations for Cfb1 and Cfb2.

To combine the FIR and the IIR network and implement the filter topology presented in Figure 5-5, we merge the moving average capacitances of Figure 5-3 and then charge transferring of the inverting integrator (Figure 5-8):

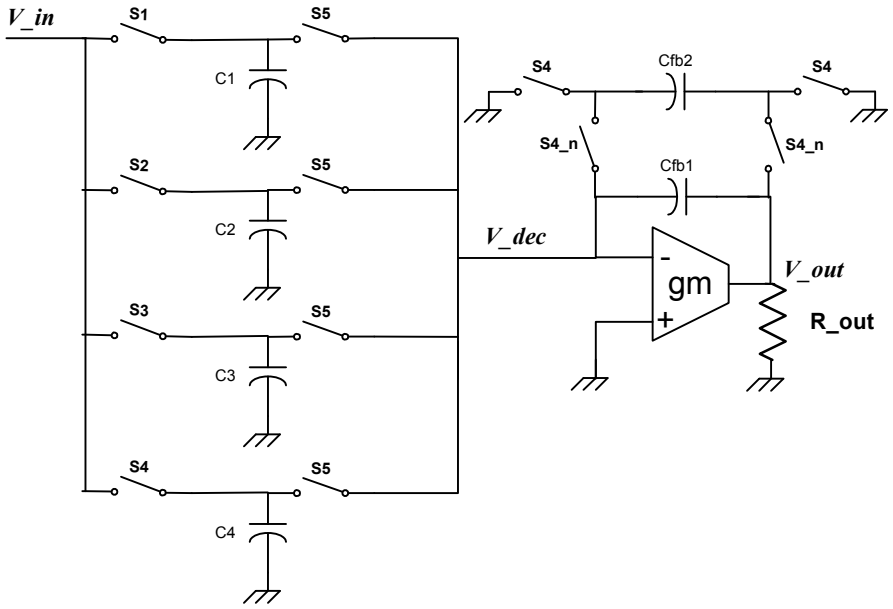


Figure 5-9 : Basic analog IIR Block Diagram

The same clock strategy presented on Figure 5-4 is applied. Just before the charge sharing on S5, Cfb2 is reset on S4, in order to reduce to β the feedback coefficient. In all other instants Cfb1 and Cfb2 are connected together. From Figure 5-9, the TF between V_dec and V_in is set by (5-5). The sum of the capacitors C1 to C4 represents CA on Figure 5-8. Finally, combining (5-5) with (5-12), we obtain:

$$H(z) = -\frac{\sum_n Cn}{Cfb1 + Cfb2} \cdot \frac{\left[C1 + C2 \cdot \left(z^{-1}\right) + C3 \cdot \left(z^{-2}\right) + C4 \cdot \left(z^{-3}\right)\right]}{\sum_n Cn \cdot 1 - \beta \cdot z^{-4}} \tag{5-13}$$

We derive the filter coefficients from the capacitor values:

$$b_n = -\frac{\sum_n Cn}{Cfb1 + Cfb2} \cdot \frac{Cn}{\sum_n Cn} \qquad \beta = \frac{Cfb1}{Cfb1 + Cfb2} \tag{5-14}$$

2.4 Complex discrete time filtering - Hilbert Transform

The discrete time filter can also be used to implement image filtering (CHAPTER 4). The frequency response of the proposed filter is asymmetric in terms of negative and positive frequencies, where the image signal is filtered. A real signal is composed single dimension; the signal *Fourier Transform* (FT) is symmetric in terms of negative and positive frequencies. The same way, a real filter is only composed by real coefficients, presenting a symmetric frequency response. In order to have complex signals or filters where the spectra are not symmetric, the Hilbert transform is applied [21]:

$$x_C[n] = x_r[n] + jx_i[n] \tag{5-15}$$

The signal contains two dimensions $x_r[n]$ and $x_i[n]$, and the *Discrete Fourier Transform* (DFT) is given by:

$$X_C\left(e^{j\omega}\right) = X_r\left(e^{j\omega}\right) + jX_i\left(e^{j\omega}\right) \tag{5-16}$$

The image frequency filtering is obtained when one of the sides (negative or positive) of $X_C(e^{j\omega})$ spectrum is different from the other half. Now consider that $X(e^{j\omega})$ a real signal which is filtered by a complex filter, the real and imaginary parts on the output are obtained by:

$$X_C\left(e^{j\omega}\right) = H_r\left(e^{j\omega}\right)\cdot X\left(e^{j\omega}\right) + jH_i\left(e^{j\omega}\right)\cdot X\left(e^{j\omega}\right) \tag{5-17}$$

On the discrete time domain, this means that from a real signal x[n], filtered by two distinct filters $H_r(e^{j\omega})$ and $H_i(e^{j\omega})$, it is possible to obtain a non-symmetric complex signal $x_C[n]$. Now we consider the real DT filter with frequency response $H(e^{j\omega})$, in order to shift the filter response, the frequency variable is substituted $\omega \rightarrow \omega - \omega_0$ [21]:

$$e^{j(\omega)} \rightarrow e^{j(\omega-\omega_0)} \tag{5-18}$$

$$\begin{aligned} z^{-n} &= e^{-j\omega nT_S} \\ e^{-jnT_S(\omega-\omega_0)} &= z^{-n}\cdot e^{jn\omega_0 T_S} \end{aligned} \tag{5-19}$$

To illustrate the frequency shifting, we consider the TF from (5-9), the chosen frequency shift is $\omega_0 T_S = \pi/2$. The relation of (5-19) is applied on (5-9):

$$H_C(z) = \frac{b_1\cdot z^{-0}\cdot e^{0} + b_2\cdot z^{-1}\cdot e^{j\omega_0 T_S} + b_3\cdot z^{-2}\cdot e^{j2\omega_0 T_S} + b_4\cdot z^{-3}\cdot e^{j3\omega_0 T_S}}{1-\beta\cdot z^{-4}\cdot e^{j4\omega_0 T_S}} = H_r(z) + jH_i(z) \tag{5-20}$$

$$H_C(z) = \frac{b_1 + j\cdot b_2\cdot z^{-1} - b_3\cdot z^{-2} - j\cdot b_4\cdot z^{-3}}{1-\beta\cdot z^{-4}} = H_r(z) + jH_i(z) \qquad b_n = 1$$

$$\begin{aligned} H_r(z) &= \frac{b_1 + b_3\cdot z^{-2}}{1-\beta\cdot z^{-4}} \\ H_i(z) &= \frac{b_2\cdot z^{-1} - b_4\cdot z^{-3}}{1-\beta\cdot z^{-4}} \end{aligned} \tag{5-21}$$

In a real implementation $H_r(z)$ and $H_i(z)$ can be two distinct real TFs and j is a phase shift operator, therefore the complex filter $H_c(z)$ is illustrated as follows:

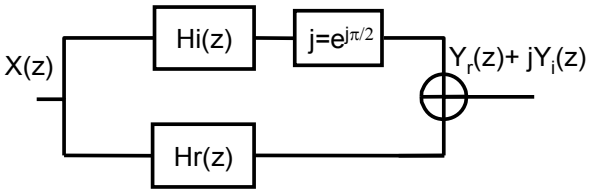


Figure 5-10 : Block diagram of image rejection complex filter ([21])

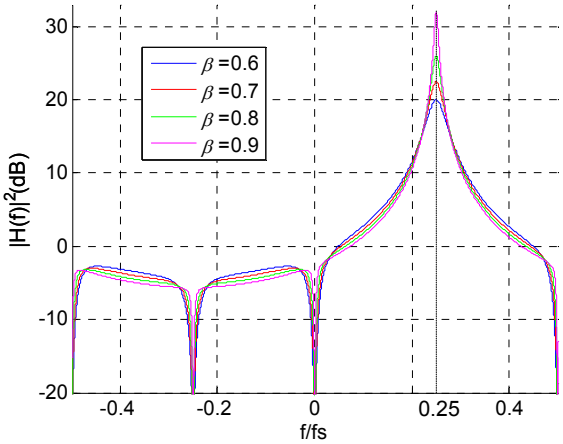


Figure 5-11 : Gain vs f/fs for the complex IIR filter

2.4.1 Analog implementation of the complex filter

As explained in the previous section, the complex filter structure is implemented by two different real DT filters $H_r(z)$ and $H_i(z)$. Since the filter is applied in discrete time, the frequency shift is not implemented by classical polyphase structure [122]. Instead the frequency shift can be implemented through the Hilbert transform. We apply the basic structure of Figure 5-9 in order to implement $H_r(z)$ and $H_i(z)$:

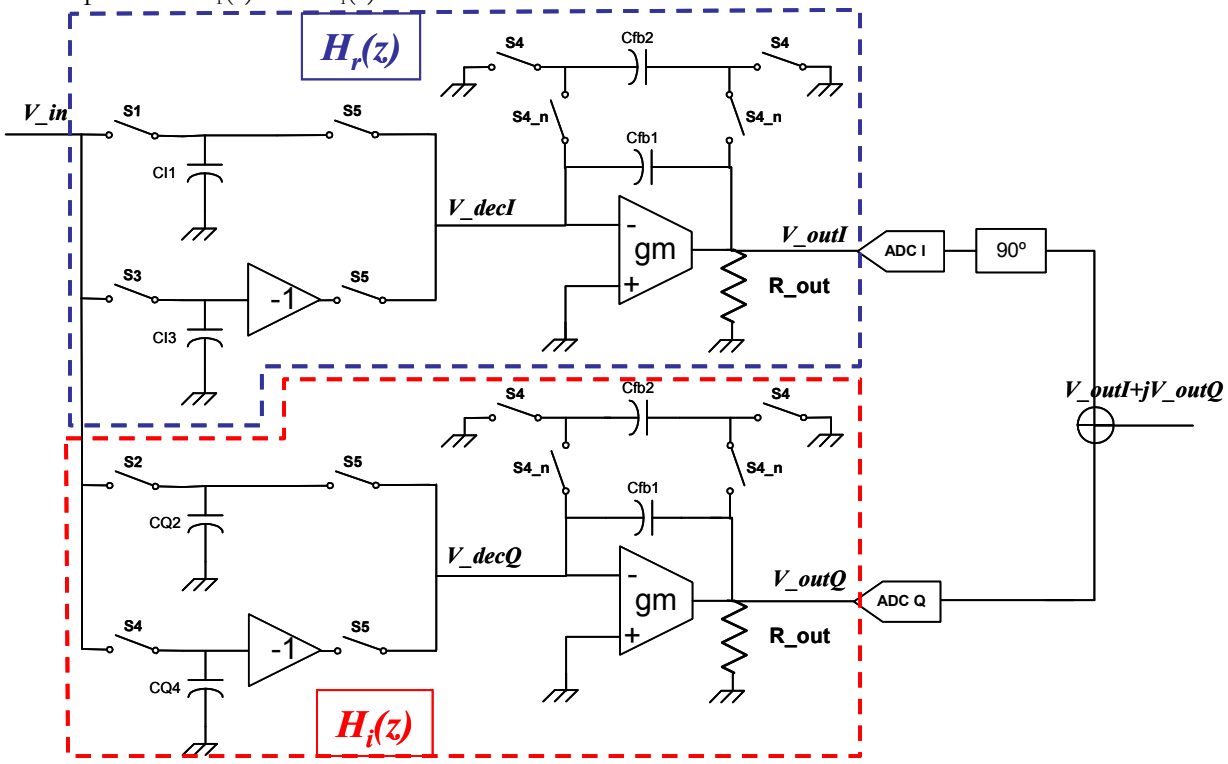


Figure 5-12 : Block diagram of image rejection complex filter

From (5-21) we observe that the complex transfer function can be separated in two real transfer functions $H_i(z)$, where odd coefficients are equal to zero, and $H_r(z)$, where even coefficients are equal to zero. The complex TF is verified in digital domain after decimation. Since the method of frequency shift consists on creating complex coefficients, but not changing the sampling clocks, the same clock strategy presented on Figure 5-4 is still applied. Negative

signs can be implemented by inverting the capacitor polarity on the charge sharing stage. In Figure 5-12 it is just represented by a "-1" gain. Based on (5-13), the TFs $H_r(z)$ and $H_i(z)$ of (5-21), become:

$$H_r(z) = -\frac{1}{Cfb1+Cfb2}\cdot\frac{\left[C1 - C3\cdot z^{-2}\right]}{1-\beta\cdot z^{-4}} \qquad (5\text{-}22)$$

$$H_i(z) = -\frac{1}{Cfb1+Cfb2}\cdot\frac{\left[C2\cdot z^{-1} - C4\cdot z^{-3}\right]}{1-\beta\cdot z^{-4}}$$

We derive the filter coefficients from the capacitor values:

$$b_n = -\frac{\sum_n Cn}{Cfb1+Cfb2}\cdot\frac{Cn}{\sum_n Cn} \qquad \beta = \frac{Cfb1}{Cfb1+Cfb2} \qquad (5\text{-}23)$$

2.5 Implementation of the proposed complex IIR filter

The proposed architecture of CHAPTER 4 based in a DT filtering network is applied before the ADC when the signal is at IF2, and after decimation, is down-converted to a low-IF IF3. The proposed filter is spectrally asymmetric, in order to filter image signals and to implement the complex down-conversion and demodulation. The last IF3 is defined as IF3=f_{ADC}/4, since this choice eases the down-conversion to the base band (1,0,-1,0 coefficients on the digital mixer). The use of a low-IF avoids the problems of DC offset, IIP2 and 1/f noise. According to the proposed frequency plan, the signal is down-converted to IF2=fs/4+fs/16 on the BPS process. Differently to the literature, where the complex DT filter is centered at fs/4 (state of the art of CHAPTER 2), the DT filter center frequency is set to IF2. The filtering network also implements the decimation by four of the discrete signal, f_{ADC}=fs/4, where the signal is down-converted to IF3=fs/16=f_{ADC}/4. Interferers can be present at multiples of f_{ADC}, which aliases within the signal of interest. Therefore, the filtering function proposed on Figure 5-6 fits with the application, since the notches are placed on multiples of the decimated frequency and the filter selectivity reduces the required dynamic range for the ADC. The filter of Figure 5-6 shifted in frequency to IF2.

The frequency shift method is presented in section 2.4. Since the required center frequency is IF2=fs/4+fs/16, we set $\omega_0 Ts=\pi/2+\pi/8$. Applying the given frequency shift on (5-9), we obtain:

$$H_C(z) = \frac{1 + z^{-1}\cdot e^{-j\left(\frac{\pi}{4}+\frac{\pi}{8}\right)\cdot 1} + z^{-2}\cdot e^{-j\left(\frac{\pi}{4}+\frac{\pi}{8}\right)\cdot 2} + z^{-3}\cdot e^{-j\left(\frac{\pi}{4}+\frac{\pi}{8}\right)\cdot 3}}{1-\beta\cdot z^{-4}\cdot e^{-j\left(\frac{\pi}{4}+\frac{\pi}{8}\right)\cdot 4}} \qquad (5\text{-}24)$$

$$H_C(z) = \frac{1 + (-A+Bj)\cdot z^{-1} + (-C-Cj)\cdot z^{-2} + (B-Aj)\cdot z^{-3}}{1 - j\beta\cdot z^{-4}} \qquad (5\text{-}25)$$

$$b_1 = 1+0j \quad b_2 = (-A+Bj) \quad b_3 = (-C-Cj) \quad b_4 = (B-Aj) \qquad (5\text{-}26)$$

A=0.3827 B=0.9239 C=0.7071

We derive the outputs for the real and the imaginary paths:

$$H_C(z) = \frac{V_{out}I + jV_{out}Q}{Vin} = \frac{b_1 + b_2 \cdot z^{-1} + b_3 \cdot Z^{-2} + b_4 \cdot z^{-3}}{1 - j\beta \cdot z^{-4}} \quad (5\text{-}27)$$

$$(V_{out}I + jV_{out}Q) \cdot (1 - j\beta \cdot z^{-4}) = Vin \cdot (b_1 + b_2 \cdot z^{-1} + b_3 \cdot z^{-2} + b_4 \cdot z^{-3}) \quad (5\text{-}28)$$

Separating real and imaginary parts:

$$V_{out}I = Vin \sum_n re(b_n) \cdot z^{-n+1} - V_{out}Q \cdot \beta \cdot z^{-4} \quad (5\text{-}29)$$

$$V_{out}Q = Vin \sum_n im(b_n) \cdot z^{-n+1} + V_{out}I \cdot \beta \cdot z^{-4} \quad (5\text{-}30)$$

As indicated on section 2.4.1, the j operator is implemented in digital domain. The j operator on the denominator of (5-27) means that $V_{out}Q$ is used on the feedback of $V_{out}I$ and vice-versa, as observed in (5-29) and (5-30). Differently to the filter presented in 2.4.1, in the proposed complex filter all samples are used on both paths. The equivalent frequency response is as follows:

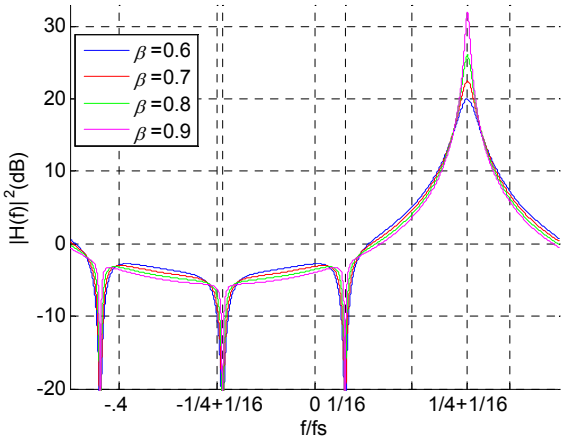


Figure 5-13 : Gain vs f/fs for the complex IIR filter

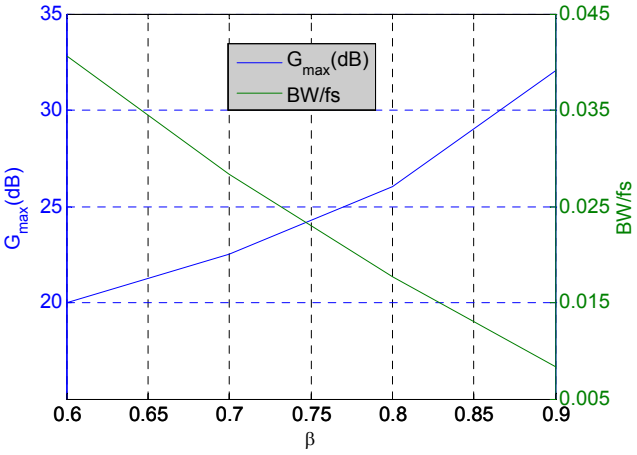


Figure 5-14 : G_{max} and BW/fs vs β

2.5.1 Analog implementation of the complex filter

The implementation of the proposed filter is based on the network illustrated on Figure 5-12. From the architecture exposed on CHAPTER 4, the continuous time IF1 filter has been chosen to be a differential structure. The filter charge is two capacitors connected to ground, composing therefore Vin+ and Vin-. The FIR stage capacitors on $H_r(e^{j\omega})$ +j·$H_i(e^{j\omega})$ are therefore doubled.

The FIR stage is illustrated in Figure 5-15. The coefficients from (5-29) are implemented by CI1 to CI4. For negative coefficients, CIn- is inverted with CIn+ on the decimation. Since the imaginary part of b1 on (5-30) is equal to "0", there are two CQ1, one is connected to the input to balance the charges with Cs and another to balance the charges on the output. From S1 to S4, the charge stored on Cs is shared with CIn+CQn, which is approximately constant for all n:

$$V_{\_balanced} = \frac{Cs}{CIn + CQn} V\_in \cdot z^{-n} = G1 \cdot V\_in \cdot z^{-n} \qquad n = [1,2,3,4] \quad (5\text{-}31)$$

The TFs $H_{r\_FIR}(z)$ and $H_{i\_FIR}(z)$ on the FIR stage are therefore derived:

$$H_{r\_FIR}(z) = \frac{G1}{\sum_n CIn} \cdot \sum_n \left[CIn \cdot sign(n) \cdot z^{-(n-1)} \right] \quad n = [1,2,3,4] \tag{5-32}$$

$$H_{i\_FIR}(z) = \frac{G1}{\sum_n CQn} \cdot \sum_n \left[CQn \cdot sign(n) \cdot z^{-(n-1)} \right] \quad n = [2,3,4] \tag{5-33}$$

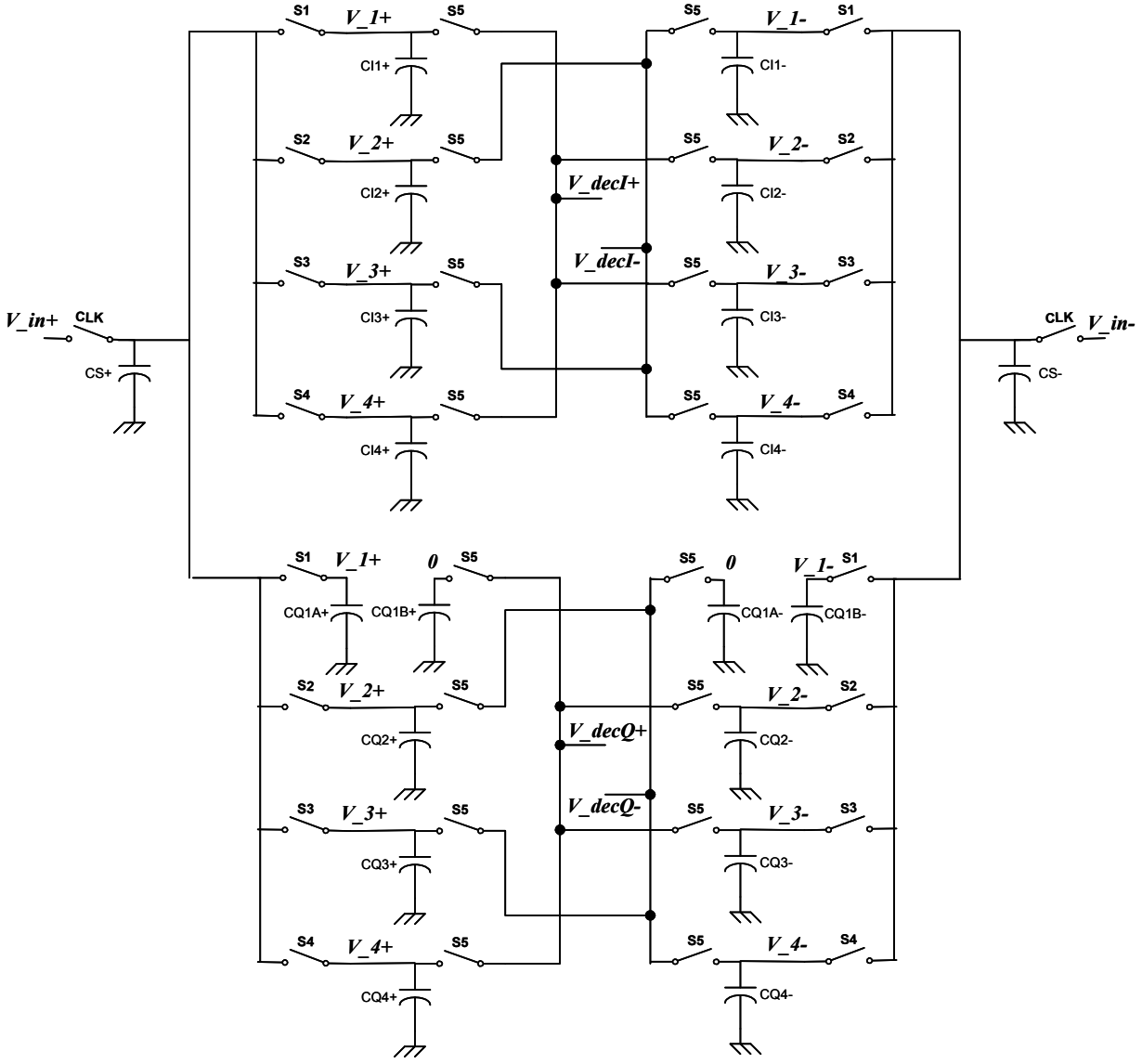


Figure 5-15 : FIR stage block diagram for the proposed filter

From (5-32) and (5-33), and from the derived $re(b_n)$ and $im(b_n)$ on (5-26), the weights between the capacitors CIn and CQn are calculated:

$$1 = CI1 \quad A = CI2 \quad C = CI3 \quad B = CI4$$
$$B = CQ2 \quad C = CQ3 \quad A = CQ4 \tag{5-34}$$

For the IIR stage, the inverse of Q path output is used on the I path TF (5-29) and the output of I is used on the Q path TF (5-30). The feedback loop schematic is implemented as follows:

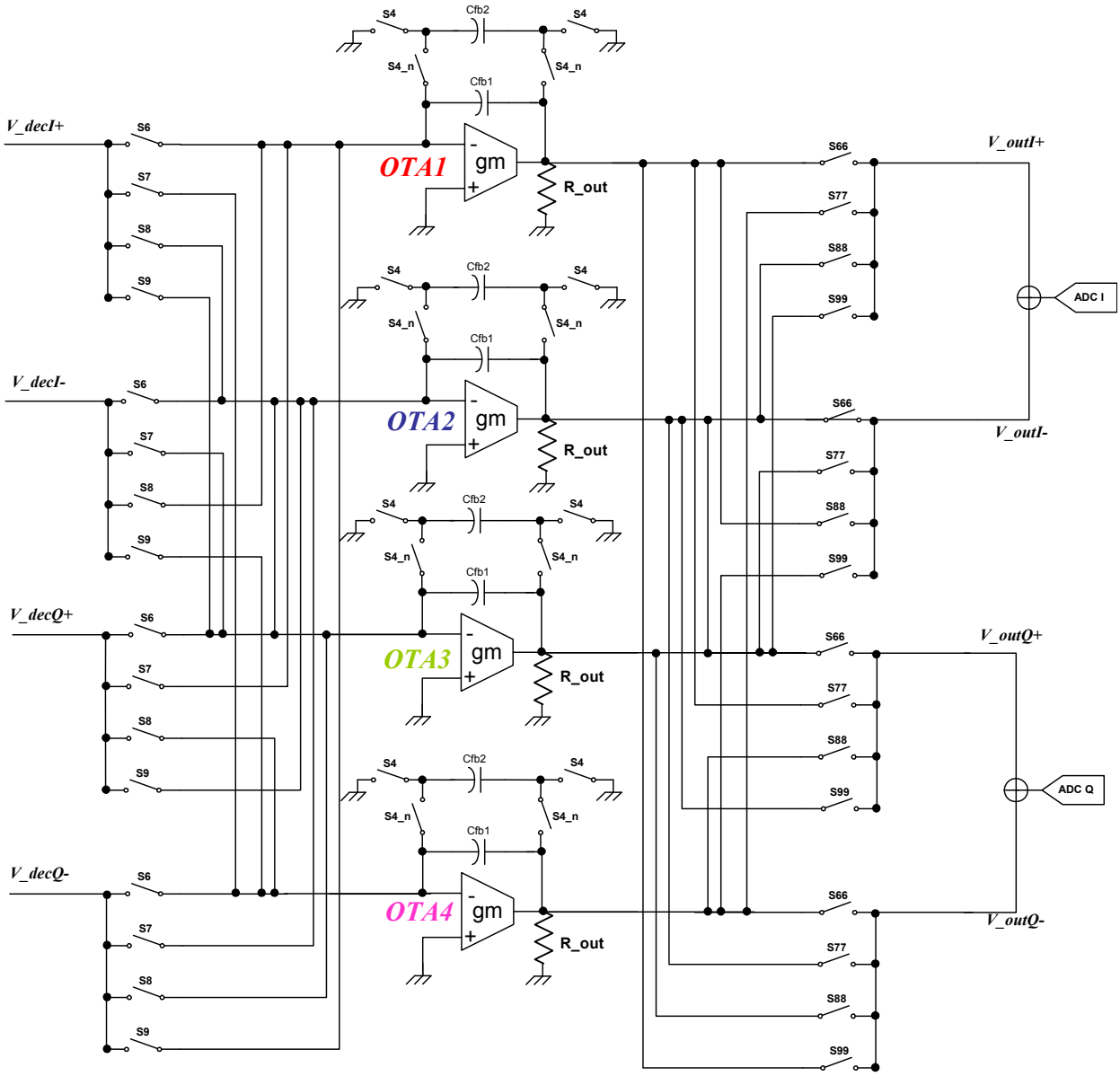


Figure 5-16 : IIR stage block diagram for the proposed filter

There are four OTA, one per path per sign. Table 5-1 summarizes the connections and the clock phases for the feedback loop:

	OTA_1	OTA_2	OTA_3	OTA_4
S6	V_decI+	V_decI-	V_decQ+	V_decQ-
S7	V_decQ+	V_decQ-	V_decI-	V_decI+
S8	V_decI-	V_decI+	V_decQ-	V_decQ+
S9	V_decQ-	V_decQ+	V_decI+	V_decI-

Table 5-1 : The connection schematics on the OTAs' input

The clocks S6 to S99 of Figure 5-16 are summarized below:

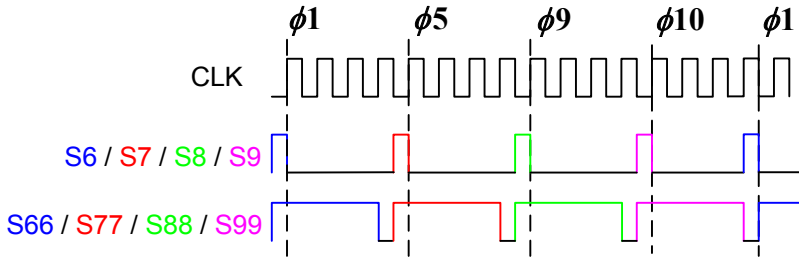


Figure 5-17 : Clock strategy for the IIR feedback stage

The clocks S66-S77 are longer in order to access an ADC which sampling frequency is fs/4. We remind the closed loop gain and feedback coefficient from (5-12):

$$\frac{V_{out}(z)}{V_{dec}(z)} = -\frac{CA}{Cfb1 + Cfb2} \cdot \frac{1}{1 - \beta \cdot z^{-1}}$$

$$\beta = \frac{Cfb1}{Cfb1 + Cfb2}$$

From Figure 5-16 we derive the closed loop gain and the feedback coefficient:

$$\frac{V_{out}(z)}{V_{dec}(z)} = -\frac{\sum_n CIn}{Cfb1 + Cfb2} \cdot \frac{1}{1 - \beta \cdot z^{-1}} = -\frac{\sum_n CQn}{Cfb1 + Cfb2} \cdot \frac{1}{1 - \beta \cdot z^{-1}} \qquad (5\text{-}35)$$

$$\beta = \frac{Cfb1}{Cfb1 + Cfb2}$$

In order to avoid I /Q gain mismatch the sum of CIn and CQn are equal, from Figure 5-15 CQ1B is calculated in order to guarantee this balance on the decimation charge sharing step. The image rejection is therefore completed in the digital domain, as the 90° phase shift is implemented (Figure 5-10). After decimation, the signal of interest is at a low-IF, IF3=f_{ADC}/4. This configuration eases the digital mixing operation to base band, since it is simply implemented by the sequence [1 0 -1 0]. The image rejection can be merged with the mixing operation to base band when a modified WEAVER structure [22] is used. In our case, the first two mixers and filters are implemented by the IIR complex DT filter and the four down-conversion mixers are implemented in digital domain. The channel selection is implemented after down-conversion to base band where further decimation can be implemented.

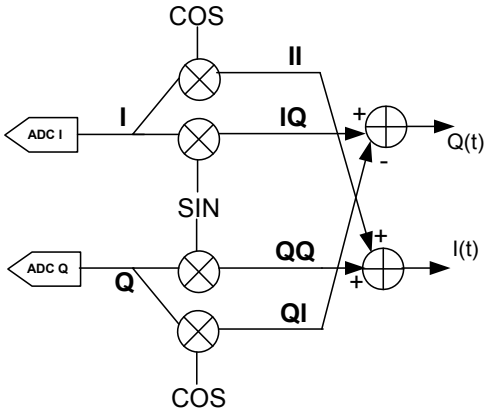


Figure 5-18 : Digital implementation of the modified WEAVER structure for demodulation and image rejection

The final TF is given by:

$$H_{rIIR}(z) = \frac{\frac{G1}{\sum_n CIn} \cdot \frac{\sum_n CIn}{Cfb1 + Cfb2} \cdot \sum_n \left[CIn \cdot sign(n) \cdot z^{-(n-1)} \right]}{1 - j \cdot \beta z^{-4}} \tag{5-36}$$

$$H_{iIIR}(z) = \frac{\frac{G1}{\sum_n CQn} \cdot \frac{\sum_n CQn}{Cfb1 + Cfb2} \cdot \sum_n \left[CQn \cdot sign(n) \cdot z^{-(n-1)} \right]}{1 - j \cdot \beta z^{-4}} \tag{5-37}$$

From (5-36) and (5-37) we derive the relations between the capacitor values and the filter coefficients of (5-25):

$$\left| re(b_n) \right| = \frac{\sum_n CIn}{Cfb1 + Cfb2} \cdot \frac{G1 \cdot CIn}{\sum_n CIn} \qquad \beta = \frac{Cfb1}{Cfb1 + Cfb2}$$

$$\left| im(b_{n(2,3,4)}) \right| = \frac{\sum_n CQn}{Cfb1 + Cfb2} \cdot \frac{G1 \cdot CQn}{\sum_n CQn} \qquad \left| im(b_1) \right| = 0 \tag{5-38}$$

From the noise specification for the sampling + filtering block derived in chapter 4 the sampling capacitor has been set Cs=800fF. For noise considerations, the sum of the filter capacitors has to be higher than the sampling capacitor:

$$\sum CIn \approx 1.2\,pF \geq Cs$$

$$\sum CQn \approx 1.2\,pF \geq Cs \tag{5-39}$$

From (5-34) the weight between the capacitors has been defined. Taking into account (5-39) the capacitor values are calculated on the FIR stage. Finally, defining β=0.8 and ΣCn/(Cfb1+Cfb2)=10, Table 5-2 summarizes the resulting filter capacitor values. The frequency response of the TF $H_{rIIR}(z)+jH_{iIIR}(z)$, is given by. Compared to Figure 5-13, the notch at –fs/4+fs/16 is degraded due to a varying charge that Cs sees for CIn+CQn (5-31), therefore G1 presented in (5-38) is not constant for all coefficients.

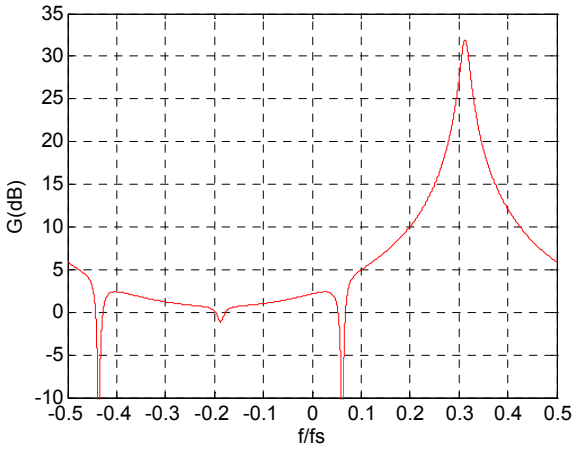


Figure 5-19 : Digital implementation of the WEAVER structure for demodulation and image rejection

	I	Q
C1	400 fF	A=200 fF - B=400 fF
C2	153.1 fF	369.6 fF
C3	282.8 fF	282.8 fF
C4	369.6 fF	153.1 fF
Cfb1	96 fF	96 fF
Cfb2	24 fF	24 fF

Table 5-2 : Summary of the filter capacitors on the FIR stag

Considering the proposed filter and the required mask of (figure 35 on CHAPTER 4), the presented frequency response respects the required specifications. The resulting TF presents 30*dB* voltage gain and IR>31dB. On the next two sections we analyze the impact on the filter performance in the presence of all these listed imperfections. The approach is either by analytical development or behavioral modeling simulations, according to the listed imperfections.

3 Analytical approach on the imperfections

3.1 Introduction to block imperfections

In section 2, an analog implementation of the proposed complex IIR filter is illustrated in Figure 5-15, Figure 5-16 and Figure 5-18. The filter implements an IIR filter which is known to have non-linear phase variations, therefore, a non-constant group delay. In this section we will quantify the distortion on the signal caused by such phenomenon. For the coefficient implementation, the derived capacitor values have to respect a certain resolution. In CMOS, the capacitors are obtained by combining a certain amount of a unit capacitance. This finite resolution changes the filter TF. The finite capacitor resolution is evaluated in this section. The unit capacitance is also linked to the capacitor mismatch variance which is related to random variations at the implementation level. The values for the components on the block deviate from the nominal one, following a certain distribution and variance. This variation also impacts the resulting TF. The filter performance is evaluated for a given variation. Variations on the OTA gain, on the capacitor mismatch, and mismatches between I and Q path are analyzed.

An ideal assumption on the charge transfers is made. The switches are considered ideal and no parasitic is considered on the system. One of the points to analyze in order to validate the filtering network is the impact of parasitic capacitances on the derived TF. In the case where the OTA presents a non-infinite gain, it also impacts the TF. Components inside the filtering network may behave non-linearly. The equivalent sampler and filter IIP3 is another characteristic of the block to put in evidence. Finally we implement an analysis on the noise generated by such structure.

3.2 IIR Group delay impact on the EVM

The filter network and TF have been defined in the previous sections. The resulting filter contains an IIR. Such filters are known to present a non-linear phase variation around the filter bandwidth [7]. Consider a system with frequency response of H(jω). The group delay is defined as the derivate of the frequency response of H(jω) [7]:

$$\tau(\varpi) = -\frac{d}{d\omega} \cdot \phi(H(j\omega)) \tag{5-40}$$

A non-linear phase variation around the BW leads to a non-constant group delay. This means that different frequencies may be subjected to different delays. This phenomenon causes inter-symbol distortion, therefore it decreases the *Signal to Noise plus Distortion Ratio* (SNDR). Linear phase filtering leads to constant group delay which avoids such source of distortion. In

this section is presented the phase response of an IIR filter and its impact in terms of signal distortion. We remind the designed filter of section 2.5 and β=0.8:

$$H_C(z) = \frac{1 + (-A + Bj)\cdot z^{-1} + (-C - Cj)\cdot z^{-2} + (B - Aj)\cdot z^{-3}}{1 - j\beta \cdot z^{-4}} \quad (5\text{-}41)$$

A=0.3827 B=0.9239 C=0.7071

We apply a zoom on the filter gain around the filter center frequency in Figure 5-20 and in Figure 5-21 we present the filter group delay around the center frequency.

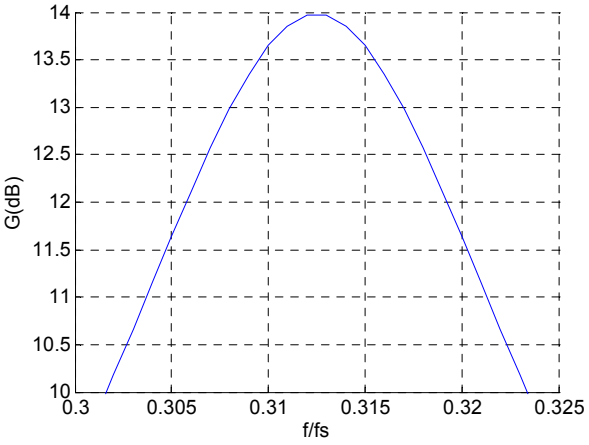


Figure 5-20 : Gain vs f/fs for the proposed complex IIR filter

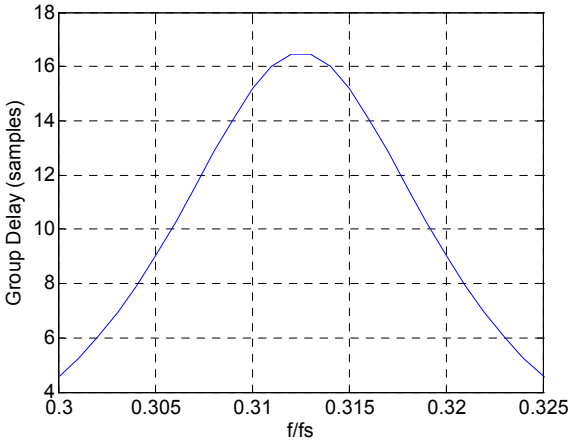


Figure 5-21 : Group delay vs f/fs for the proposed complex IIR filter

The filter -3dB BW=0.02·fs. From Figure 5-21 the group delay varies from 16.2 to 7.5 samples around the center frequency, which imposes a careful study on the impact on the signal error vector magnitude (EVM). The test bench to evaluate the distortion after filtering is defined as follows: first we generate modulated signals following the IEEE802.15.4 and BlueTooth Low Energy standards centered at IF2, which is filtered and demodulated. The ideal constellation is compared to the filtered one. The resulting EVM and therefore the *Signal to Distortion Ratio* (SDR) are derived for different IIR filter bandwidths. First, we remind the definition of EVM [123]:

$$EVM_{RMS} = \frac{\frac{1}{N}\sum_{n=1}^{N}\left|S_n - S_{0,n}\right|^2}{\frac{1}{N}\sum_{n=1}^{N}\left|S_{0,n}\right|^2} \quad (5\text{-}42)$$

where S_n is the normalized n^{th} symbol in the filtered constellation, $S_{n,0}$ is the ideal normalized constellation point of the n^{th} symbol and N is the number of unique symbols in the constellation. Then, the SDR can be related to the EVM through the following equation [123]:

$$SDR \approx \frac{1}{EVM^2} \quad (5\text{-}43)$$

The resulting SDR depends on the signal and on the filter bandwidths. For different β varying from β=0.6 to 0.9 we evaluate the group delay and the resulting SDR for IEEE802.15.4 and BT-LE signals. The applied sampling frequency is fs=98MHz (frequency plan for the proposed architecture in CHAPTER 4).

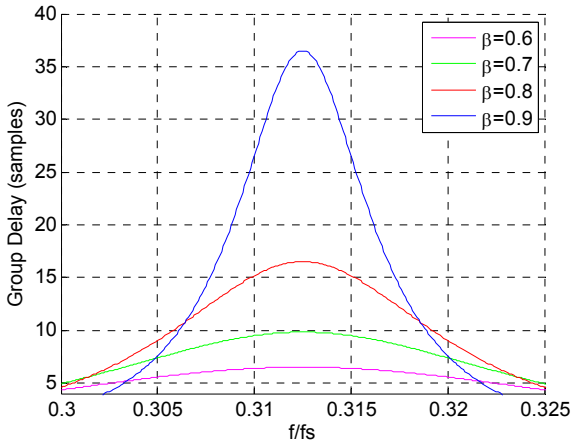


Figure 5-22 : Filter group delay for different β

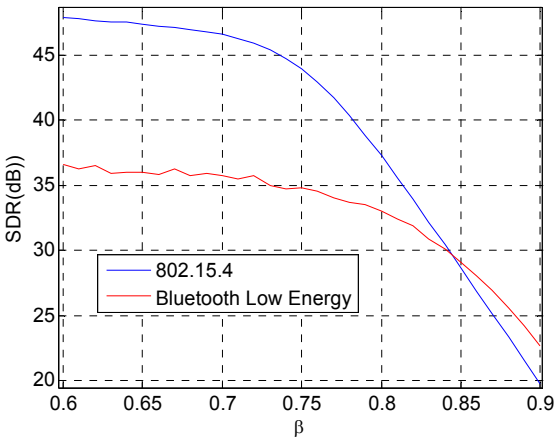


Figure 5-23 : SDR vs β

We presented in CHAPTER 4 that the more selective the IIR filter, the more relaxed the ADC specifications in terms of dynamic range. On the other hand, the filter distortion becomes a constraint. We remind from CHAPTER 3 that the minimum required SNDR for ideal non-coherent demodulation is 10dB for BT-LE and 0.5dB for IEEE802.15.4. Taking into account the SNDR degradation distribution presented in CHAPTER 4, the allowed SNDR at the VGA output (the VGA is the IIR OTA) is SNDR=20dB for BT-LE (block $B4_3$ on figure 52 of CHAPTER 4) and SNDR=6dB for IEEE802.15.4 (block $B4_3$ on figure 53 of CHAPTER 4). Considering the resulting SDR on Figure 5-23 for β=0.8, the non-linear phase distortion represents 5% of the total allowed SNDR for BT-LE and 0.08% for IEEE802.15.4. We observe a rejection of 12dB @ f/fs=0.0306 away from the center frequency. For a sampling frequency of fs=98MHz, it represents 3MHz, the distance between the signal of interest and the strongest close interferer defined for the BT-LE (table 6 of CHAPTER 3). The applied β is β=0.8. This means a gain of 2 bits on the ADC level.

3.3 Impact of the filter coefficients finite resolution and the unit capacitance definition

The equivalent IIR TF has been defined in (5-36) and (5-37). The impact of finite resolution on DT digital filters is presented in [7]. In our application, the proposed analog IIR filter also presents finite resolution coefficients. This is due to technological limits on the implementation of different capacitor values. This limitation is due to layout implementation [124]. The layout issues are linked to the nominal capacitance variation. According to [124], good matching is achieved by combining multiple unit capacitors to compose the aimed capacitance. Those unit capacitors should present the same surface and shape (form factor) in order to improve the matching. To further improve the matching, the applied unit capacitor has to be relatively high to reduce fringing effect. The higher the unit capacitor, the smaller the mismatch σ(%), therefore the mismatch parameter η is defined is given as follows:

$$\sigma(\%) = \frac{\eta}{\sqrt{C_u(fF)}} \cdot \frac{1}{100} \tag{5-44}$$

We remind capacitor values summarized in Table 5-2 for the FIR stage:

	I	Q
C1	400 fF	A=200 fF – B=400 fF
C2	153.1 fF	369.6 fF
C3	282.8 fF	282.8 fF
C4	369.6 fF	153.1 fF

Table 5-3 : Summary of the filter capacitances for the FIR stage

	I	Q
C1	400 fF	A=200 fF - B=400 fF
C2	150 fF	350 fF
C3	300 fF	300 fF
C4	350 fF	150 fF
Cfb1	100fF	
Cfb2	20fF	

Table 5-4 : Summary of the filter capacitances, Cu=50fF for the FIR stage and Cu_fb=20fF for the feedback capacitors.

From the real part of the filter coefficients the capacitor values are derived for the in-phase path and from the imaginary part of the filter coefficients we derive the values for the quadrature path capacitors. The capacitances from Table 5-3 are applied on equations (5-36) and (5-37). The derived coefficients are rounded and the resulting filter presents a different TF from the nominal one. A unit capacitor for the FIR stage is chosen respecting a trade-off between coefficient implementation resolution and capacitance mismatch (which is presented in section 3.4.1). For the feedback capacitors, the defined unit capacitance is C_{u_fb}=20fF (Cfb1=100fF and Cfb2=20fF), which leads to a β=0.833 still acceptable on the filter (Figure 5-23). According to ST CMOS 65nm technology the lowest achievable capacitance is 8fF. The following figures show the derived TFs for unit capacitors equal to C_u=25fF, C_u=50fF, C_u=100fF:

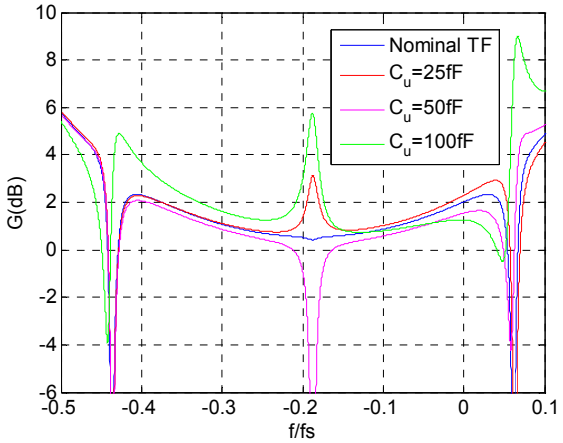


Figure 5-24 : IIR TF around the zeros

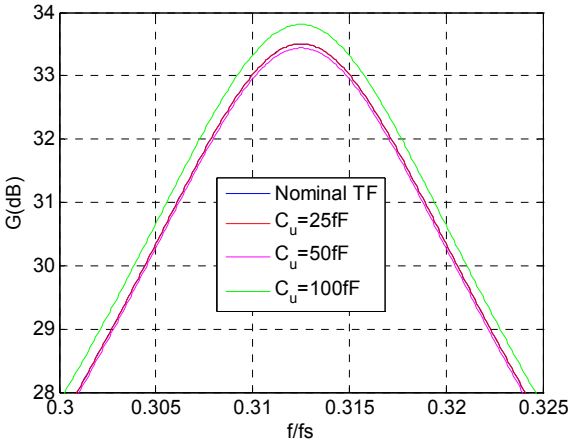


Figure 5-25 : IIR TF around the pole

From Figure 5-24, we verify that the unit capacitance is 50*fF* and presents very few deviations from the nominal TF. From the non-constant G1 observed in (5-36) and (5-37), the unit capacitance of C_u=50fF actually improves the notch at the image frequency (Figure 5-24). On the pass-band (Figure 5-25), we observe no shift in frequency, gain losses come from differences on the first charge sharing stage G1 (5-31). The next section shows how important is the choice of a relatively high unit capacitance, since we evaluate the impact of the capacitor value variations on the TF. The derived capacitances for the block implementation are summarized as follows:

3.4 Impact of the technological dispersion on the TF

On the previous section, the capacitors values have been defined in order to implement the required IIR filter TF. Section 2.3.1 has shown how the feedback loop for the IIR filter is implemented applying an OTA and the two feedback capacitors Cfb1 and Cfb2. In this section we analyze the robustness of the filter in the case of technological dispersion on these two main blocks: the capacitor values and the OTA open-loop gain.

3.4.1 Capacitance mismatch

In this section we evaluate the performance of the proposed IIR filter in section 2.5.1 when coefficients deviate from their nominal values. The filter is evaluated in terms of interferers and image rejection. With respect to the TF derived in section 2.5.1, the aliasing interferers are located at -7·fs/16 and fs/16, and the image signal at -3·fs/16 (as defined in figure 35 of CHAPTER 4). The rejection is evaluated around these frequencies considering the BT-LE BW_{CH}=1.25MHz. The applied sampling frequency is fs=100MHz. A Monte Carlo study is carried out in MATLAB considering the capacitors of Table 5-4. The nominal TF is derived in section 2.5.1. On the following, we illustrate the mean and worst case, the mean minus three times the standard deviation (μ-3σ) for the interferers and the image rejection for a given capacitance mismatch.

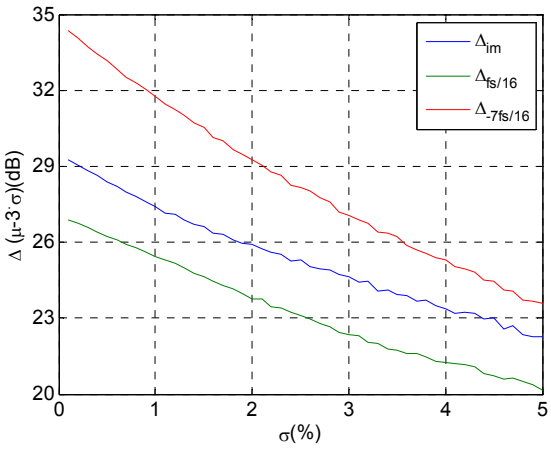


Figure 5-26 : Rejection for worst case (μ-3σ) for the critical frequencies (aliasing and image)

We observe that the filter worst interferer rejection is at fs/16. The specified image rejection (chapter 4) of 26dB is respected up to a capacitance mismatch of 2%. At that standard deviation, the lowest rejection presented is 23.7dB (for the interferer at fs/16). We remind from (figure 35 chapter 4), the required mask for that frequency is Δ_{int}=21.5dB. We target to implement the filter in ST CMOS 65nm technology, and the unit capacitance of 50fF. The capacitance mismatch reduces proportionally to the unit capacitance. From (5-44), η is defined for a given technology. for ST CMOS 65nm technology, η=1.5·√fF. Since the filter unit capacitance is C_u=50fF, the mismatch standard deviation is σ(%)=0.2% which represents the first point on the scale of Figure 5-26 and less than 0.5dB degradation on the TF performances. It is therefore concluded that the choice for the unit capacitance is largely sufficient to implement the proposed filter in ST CMOS 65nm technology.

3.4.2 OTA finite gain and gain fluctuation

For the OTA, the impact of deviations from the nominal value on the TF is mostly on the gain and on the BW of the filter. We remind from section 2.3.1 the feedback TF for an ideal OTA, presenting infinite open-loop voltage gain:

$$H(z) = K_d \cdot \frac{1}{1-\beta z^{-1}} \qquad \beta = \left(\frac{Cfb1}{Cfb2+Cfb1}\right) \qquad K_d = \frac{\sum Cn}{Cfb2+Cfb1} \tag{5-45}$$

Whenever the OTA presents a finite gain A0, the TF becomes ([125]):

$$H(z) = \widetilde{K}_d \cdot \frac{1}{1-\beta\cdot\alpha\cdot z^{-1}} \qquad \alpha = \left(1-\frac{\widetilde{K}_d}{A0}\right) \qquad \widetilde{K}_d = \frac{K_d}{1+\frac{1}{A0}(1+K_d)} \tag{5-46}$$

The feedback coefficient in relation (5-12) was only β and now it becomes β·α. The OTA open-loop voltage gain A0 is defined by a transconductance gm and an output resistance R_{out}. From the literature [ref?], the product $gm \cdot R_{out}$ may suffer from variations up to ±30%. A variation on A0 will result on a deviation for the closed loop gain G_{CL} and on the feedback coefficient β·α. The required deviation is set to 10% for G_{CL} and 3% on α, since the last is linked to the filter bandwidth. First we derive $G_{CL}(A0, K_d, \beta)$ and $\alpha(A0, K_d)$:

$$G_{CL} = \frac{A0 \cdot K_d}{(A0+1+K_d)(1-\beta)+\beta\cdot K_d} \tag{5-47}$$

$$\alpha = 1 - \frac{K_d}{A0+1+K_d} \tag{5-48}$$

We are interested in verifying the variation on G_{CL} and α related to A0 for a constant K_d and β and for which value of A0 the relative variation is lower than 10%.

$$\left|\frac{\partial G_{CL}}{\partial A0}(A0)\times dA0\right| < 10\% \quad \text{for dA0=0.3} \tag{5-49}$$

$$\left|\frac{\partial \alpha}{\partial A0}(A0)\cdot dA0\right| < 3\% \quad \text{for dA0=0.3} \tag{5-50}$$

Considering capacitor values defined in Table 5-4, K_d=10, β=0.83. In Figure 5-27 we illustrate the numerical application of (5-47) and (5-48) for different values of A0 (and considering 30% of deviation for A0) in order to find A0 which satisfies the condition of (5-49) and (5-50).

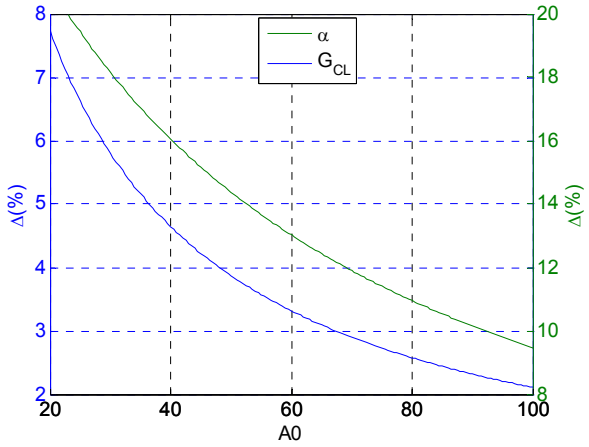


Figure 5-27 : Deviation for G_{CL} and α (%) vs A (@ deviation of 30%)

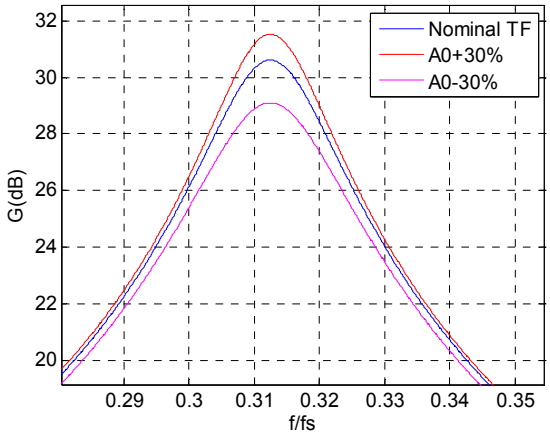


Figure 5-28 : IIR TF around the pole, A0=100.

The open-loop gain of g=100 is chosen in order to have less than 3% deviation on the feedback loop coefficient (Figure 5-27) and 10% on the closed loop gain. Such configuration permits to apply only two gain stages on the OTA in order to implement the required gain.

3.4.3 On the Agility of the IIR Filter

Equation (5-46) shows that for a constant open-loop gain A0, the closed-loop gain is dependent on the feedback capacitors and on the sum of the capacitances on the FIR stage. K_d is dependent on the sum of Cfb1 and Cfb2 and the feedback loop is dependent on the ration Cfb1/Cfb2. Considering A0=100, we illustrate different configurations of gain and bandwidth (summarized in Table 5-5)

	Cfb1 (fF)	Cfb2 (fF)	β	β·α	K_d	$\widetilde{K}_d$
TB1	100	20	0.83	0.76	10	9
TB2	70	50	0.58	0.53	10	9
TB3	480	120	0.8	0.78	2	1.94

Table 5-5 : The test benches for OTA open-loop gain impact on TF

The different test benches show that it is possible to reconfigure the closed-loop gain and the filter selectivity by changing the capacitor pairs Cfb1 and Cfb2. It is also verified that the OTA open-loop gain degrades both the gain and the filter selectivity, as illustrated below:

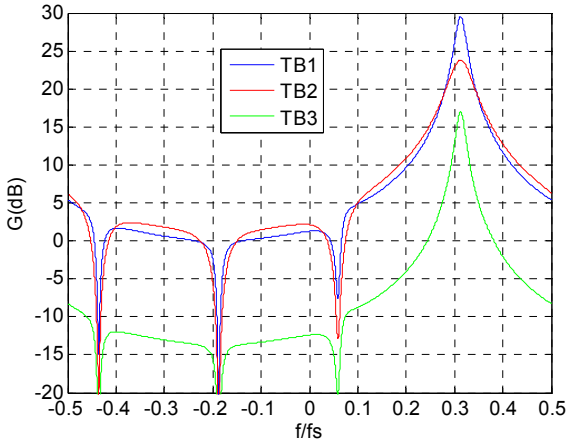


Figure 5-29 : Frequency response on the different test benches

3.4.4 I /Q gain and phase mismatch

The ideal complex demodulation considers 90º phase difference and equal gain between paths. In a block implementation, some technological mismatches can cause a static error between the paths. In a low-IF complex filtering architecture, these mismatches cause losses in the image rejection performance. In the case of the Zero-IF architecture, it causes distortions on the signal. A phase imbalance may come from a difference in the layout between paths and one technique to overcome this problem is to design the layout as symmetric as possible [126]. Some active blocks in the receiving path may also present different gains, causing I/Q gain mismatch.

Differently to complex sampling/mixing architectures (section 3.2 from CHAPTER 2), the proposed IIR complex filter uses just one clock reference. This excludes the phase mismatch coming from quadrature generated LO. The phase difference is implemented by applying the Hilbert transform on the filter TF. As discussed in 2.4 the phase shift is implemented directly on the filter coefficients. The precision on the filter capacitances defines the phase shifting. In the previous section, the effect of the capacitor mismatches on the TF has already been analyzed, including also the phase shift mismatch. The amplitude mismatch may come from differences between the paths on the active blocks, , for example, in the receiver base band amplifier. We demonstrated in section 2.5.1 that the filter's OTAs are constantly changing paths, in order to implement the complex feedback loop of equation (5-25). From Figure 5-16 we observe that the different OTA are rotating between paths. Although they may have different open-loop gains, they do not represent a static mismatch between phases, but only a variance on the gain. This means that in average the OTA gain is the same for the paths. The impact of OTA closed-loop gain variance is evaluated on 3.4.2.

On the other hand, phase and gain mismatch can occur on the sampling instants. The phase mismatch may come from the different clock path to access the I and Q sampling switches and as well from sampling jitter. The effect of the sampling jitter on the *Signal to Jitter Distortion Ratio* (SDjR) will be discussed on CHAPTER 6.

No apparent I/Q gain mismatch is observed, but we evaluate the filter performance regarding both gain and phase imbalance anyway. The gain mismatch is applied on $(1+\Delta G)re(b_n)$ of (5-38). The voltage gain varies from -10% to 10%, $0.9<(1+\Delta G)<1.1$. The phase mismatch varies from $-5^o<\varphi<5^o$ applied on $(b_n)e^{(j\,2\pi\varphi/360)}$.

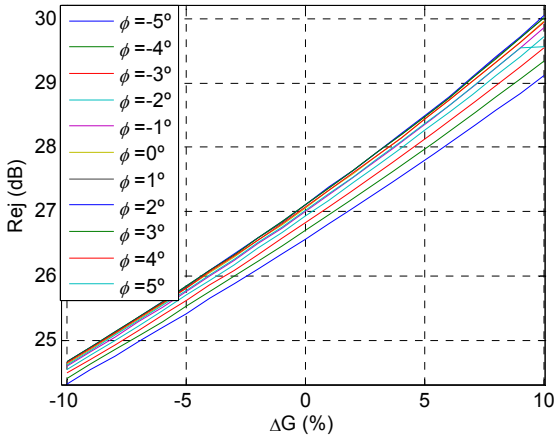


Figure 5-30 : Interferer rejection @ $fs/16$ vs G mismatch – phase mismatch from -5° to 5°

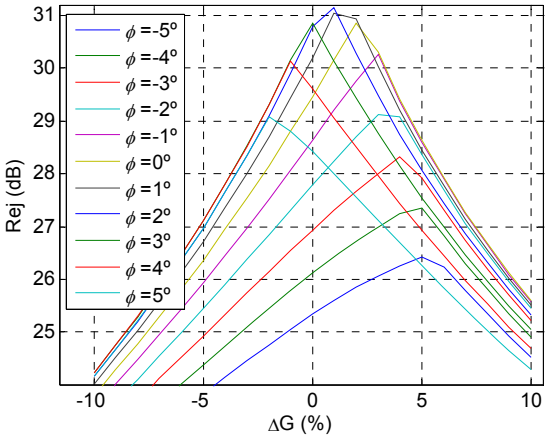


Figure 5-31 : Interferer rejection @ $-fs/2+fs/16$ vs G mismatch – phase mismatch from -5° to 5°

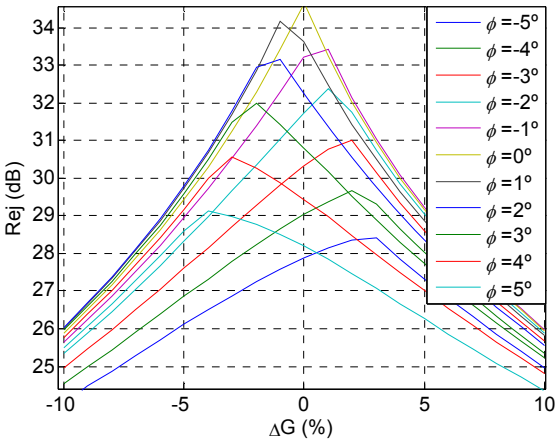


Figure 5-32 Image rejection @ $-fs/4 + fs/16$ vs G mismatch – phase mismatch from -5° to 5°

From Figure 5-32 we observe that the image rejection (26dB from CHAPTER 4) is respected in a gain and phase mismatch up to 5% and 5° respectively. From Figure 5-30 and Figure 5-31 the interferer rejection @ fs/16 and @ –fs/2+fs/16 are superior to 24dB in the same range of mismatches. In a practical case, the error coming from I/Q mismatches are combined with the capacitance mismatches. Therefore, some margins are considered from the allowed variances and mismatches.

3.5 Noise analysis

3.5.1 Analytical Approach

One major concern on a passive capacitor filtering network is the sampled thermal noise. In this section we analytically develop the filter output referred noise power spectral density. This development is based on [18] and consists on considering each of the filter switches as an independent thermal noise source. The superposition principle is therefore applied on the system in order to sum the noise powers on the output. We derived the NF for the FIR stage, since the noise of the OTA is not taken into account. From CHAPTER 3, the system design methodology defines that the NF is referred to the input and antenna impedance. In order to calculate the input referred noise for the sampler plus the FIR stage filter, the equivalent TF for the FIR stage

is derived. The TF for each noise source is derived for the FIR stage filter. From the defined filter capacitors on section 3.3 the output noise is calculated and then referred to the input. Each switch is modeled as a noise source which is low-pass filtered by the RC network; therefore the total noise power per switch-cap is KT/C. The FIR stage noise schematic is given as follows:

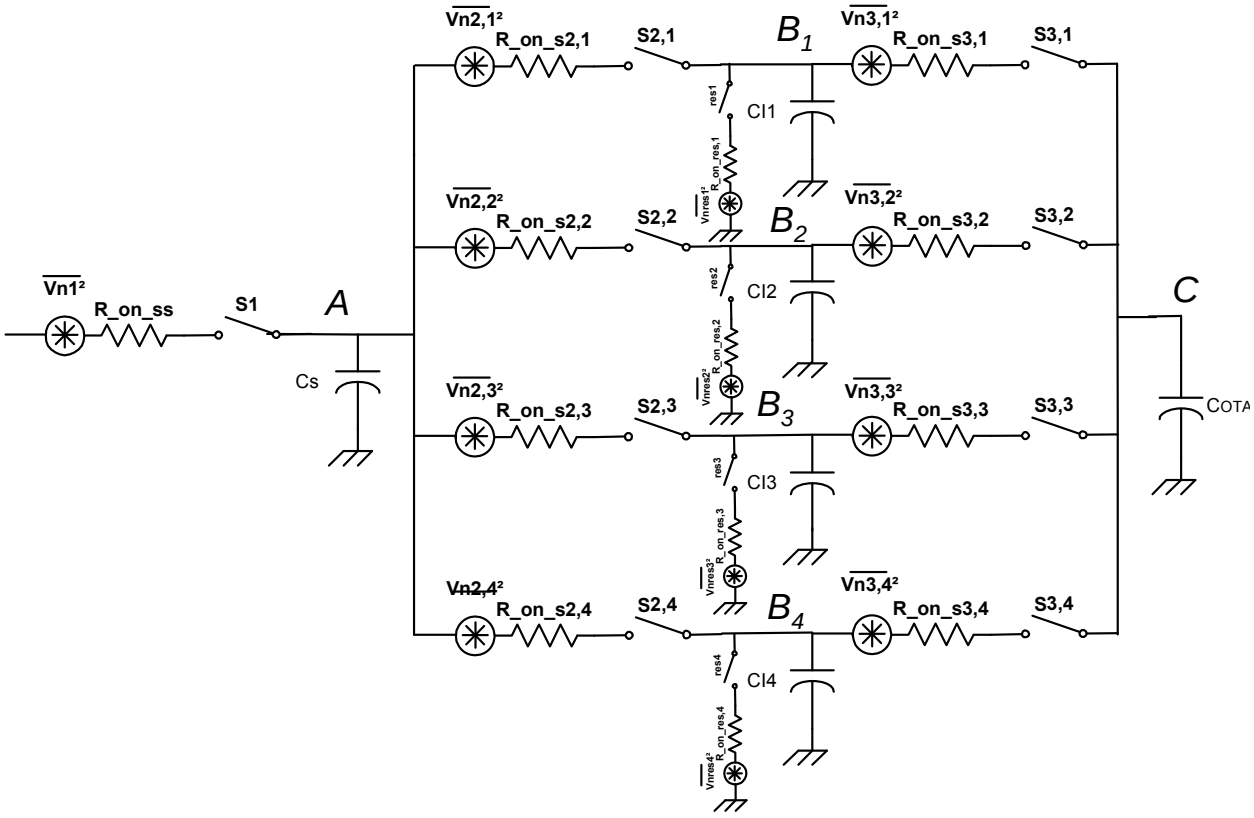


Figure 5-33 Equivalent noise schematic for the FIR stage on the I+ path

The equations that derive the output noise power on node *C* from each one of the noise sources is described in detail in APPENDIX F . The total output noise is given as follows:

$$\overline{Vn\_tot^2}_{,C} = \overline{Vn1^2}_{,C} + \overline{Vn2^2}_{,C} + \overline{Vn3^2}_{,C} + \overline{Vn_{OTA\_IN}{}^2}_{,C} \tag{5-51}$$

$$\overline{Vn1^2}_{,C} = \sum_k \left[\overline{Vn1^2}_{,Bk} \cdot \frac{C_{Ik}{}^2}{C_{TOT}{}^2} \right] \text{ with } C_{TOT} = \sum_k C_{Ik} + C_{OTA} \tag{5-52}$$

$$\overline{Vn2^2}_{,C} = \sum_k \left[\overline{Vn2,k^2}_{,Bk} \cdot \frac{C_{Ik}{}^2}{C_{TOT}{}^2} \right] \tag{5-53}$$

$$\overline{Vn2,k^2}_{,Bk} = KT \cdot \frac{1}{Cs + C_{In} + C_{Qn}} \cdot \left(\frac{Cs + C_{Qn}}{C_{In}} + \frac{C_{Qn}}{Cs + C_{In}} \right) \tag{5-54}$$

$$\overline{Vn\_res^2}_{,C} = \frac{KT}{C_{TOT}} \cdot \sum_k C_{Ik} \tag{5-55}$$

$$\overline{Vn3^2}_{,C} = KT \cdot \frac{1}{C_{TOT}} \cdot \sum_k \left(\frac{C_{Ik}}{C_{TOT} + C_{Ik}} \right) \tag{5-56}$$

The total output noise is obtained by calculating (5-51) applying the FIR filter capacitances of Table 5-4. Since the filter is differential and contains I and Q paths, the output noise is multiplied by 4. On the output the total noise is aliased to the $f_{ADC/2}$ band. The output power spectral density is given by:

$$PSD_n = \overline{Vn^2} \cdot \frac{2}{f_{ADC}} \left(V^2 / Hz \right) \tag{5-57}$$

The input referred noise considers the power transfer function for the filter. In this analysis, the IIR feedback loop is not considered; the TF is given by (5-32) and (5-33). The gain is computed G^2=-3.77dB. Considering the noise floor of Vn_{in}^2=-187dBV²/Hz (noise floor of a 50Ω resistance) and the input referred noise, the equivalent NF (dB) is given:

$$NF_{50\Omega}(dB) = 10 \cdot \log\left(\frac{PSD_n}{G^2 \cdot Vn_{in}^2} \right) \tag{5-58}$$

Table 5-6 summarizes the output PSD per noise source and the equivalent NF :

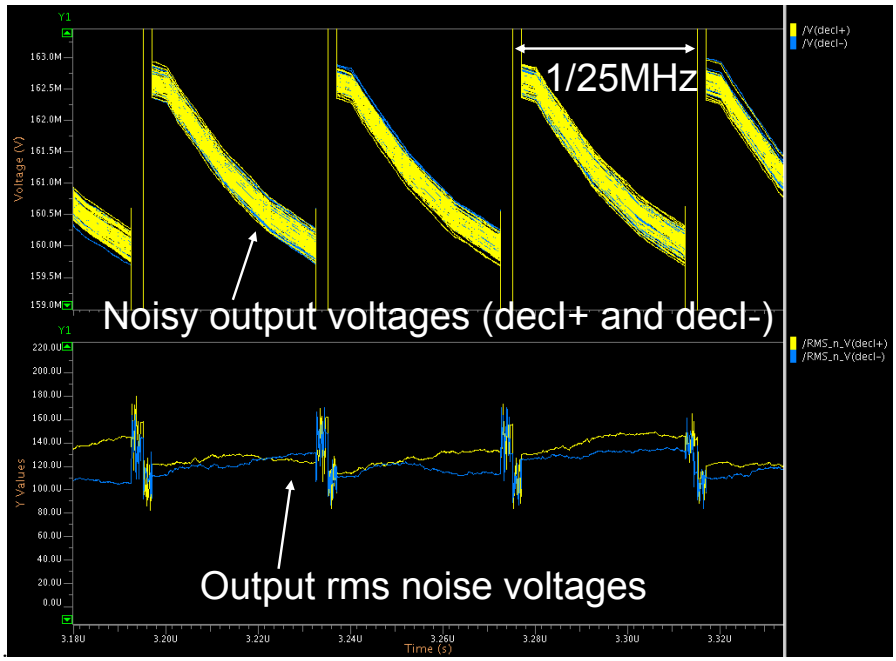
	$PSD_{n,out}$ (dBV²/Hz)	$NF_{50\Omega}$ (dB)
1	-159.3	31.5
2	-152.16	38.6
res	-151.21	39.6
3	-150.1	40.7

Table 5-6 : The test benches for OTA open-loop gain impact on TF

The equivalent NF is NF_{eq}=44.7dB. The NF coming from the averaging capacitances are around 10dB over the sampling capacitance. Compared to the expected NF for the sampler plus filter stages (block B3 on table 13 of CHAPTER 4) it becomes essential to have an amplification stage after sampling and before the filter. The gain of 12dB on the FIR stage shifts the input referred noise of the last switches to PSD3,in = -156dBV²/Hz which means an equivalent NF of 31dB, more reasonable with regards to the $SNRD_{deg}$ distribution on CHAPTER 4.

3.5.2 DT filter noise simulation and analytical approach validation

The proposed filter is currently being developed in ST CMOS 65nm technology inside the LAIR laboratory. The FIR stage is implemented and the complex transfer function is validated. Transient noise simulation is being carried out in order to evaluate the output noise and also to validate the noise model. Figure 5-34 illustrates the simulation results for the noisetrans simulation. In Figure 5-34 (a), multiple noise realizations are overlapped in order to set the standard deviation from the ideal point (the biasing voltage). We observe the filter capacitors discharges over time (the decrease of the signal in Figure 5-34 (a)), and it varies from the nominal value. In Figure 5-34 (b), we observe the standard deviation of the nominal value over time, which leads to the noise voltage RMS, the average over time for the noise RMS is V_{RMS}=115μV_{RMS} for each channel. The noise is multiplied by four considering double path differential network. Considering the last decimated frequency f_{ADC}=25MHz, the derived PSD is $PSD_{,out}$=-140dBV²/Hz and NF_{eq}=47dB. 2.3dB difference is found between simulation and theoretical analysis, which may come from flicker noise which is not taken into account on the analytical model. The analytical development allows a quick definition of the filter capacitors with reasonable precision on the equivalent NF evaluation.



(a)

(b)

Figure 5-34 Transient noise simulation, output noise RMS voltage.

4 VHDL-AMS behavioral modeling for IIR complex filter

4.1 Motivation, modeling and validation test benches

4.1.1 Motivation

The DT filtering theory has been presented and an analog filtering network based on charge sharing as well as a switching capacitor OTA has been proposed in section 2.5.1. The analytical development enables to evaluate the filter TF and the impact of some blocks imperfections on this TF. In order to validate the derived filtering network of section 2.5.1 closer to the block level, the filter has been modeled in VHDL-AMS. The block TF is validated in a SPICE environment simulation. This allows understanding the impact of more block implementation imperfections, such as parasitic capacitances. The filtering schematic is composed of three basic VHDL-AMS blocks: the switch, the OTA and the clock tree. The validation test benches are based on transient simulation. In VHDL-AMS simulations, it is possible to change blocks parameters and validate their performances faster than block simulation. The simulation is technological independent, thus parametric simulation can also help to know how technology variations can impact the required specifications. The basic block models and possible imperfections to be evaluated are presented below.

4.1.2 Models

- **Switch model**

The implemented model schematic is presented as follows:

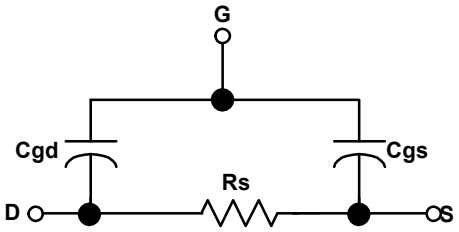


Figure 5-35 The switch VHDL-AMS model schematic

The model is basically a varying resistance R_S depending on the input voltages (V_G, V_D and V_S). The *Gate* (G), *Drain* (D) and *Source* (S) are defined on the model and interact with the exterior (the overall scheme). Whenever no voltage is presented on the gate, the transistor is on R_{off} state, therefore presenting a finite R_{off} resistance. On the conducing region, $R_S=R_{eq}$ follows a second order polynomial law in order to take into account the non-linearity effect of a switch. The second order R_{req} means a third order polynomial on the voltage transfer function. The capacitors connected to the gate C_{gs} and C_{gd} are set is inversely proportional to R_{eq} (increasing of the transistor size or number of fingers).

$$R_S = \begin{cases} R_{off} & \text{if } Vgs < 0.5 \\ R_{eq} & \text{if } Vgs > 0.5 \end{cases} \tag{5-59}$$

$$R_{eq} = \left(R_{ds} - \alpha_1 \cdot (Vcm) - \alpha_2 \cdot (Vcm)^2\right) + \alpha_1 (1 - Vgcm) + \alpha_2 \left(1 - Vgcm^2\right) \tag{5-60}$$

where $Vgcm = Vg - Vcm$

$$Vds = R_{eq} \cdot Ids \tag{5-61}$$

$$Vcm = \frac{Vd + Vs}{2} \tag{5-62}$$

$$Igs = Cgs \frac{dVgs}{dt} \tag{5-63}$$

$$Igd = Cgd \frac{dVgd}{dt} \tag{5-64}$$

where Vcm is the common mode voltage defining the biasing for R_{eq}.

The technology parameters are: Rds, Cgs and Cg, all of them proportional to the switch surface or number of fingers. From (CHAPTER 2) we observe the cut-off frequency of a S/H block. A trade-off is set between the switch-capacitor RC time constant requirements and the amount of the parasitic capacitances. On the filtering network, these parasitic capacitances store a part of the sampled charge, changing the filter TF. One test bench in this section consists on applying different parasitic capacitances in order to analyze the impact on the filter transfer function. The complete code is in APPENDIX D .

- **OTA model**

The application of an Operational Transconductance Amplifier to implement the IIR TF has been defined in section 2.3.1. This block, in addition to a capacitive feedback loop, implements the filter denominator coefficient β (5-12). Prior to the ADC, this block also implements the last gain stage, which represents the *Variable Gain Amplifier* (VGA) presented in chapter 4. The filter gain is reconfigurable by changing the Cfb1+Cfb2 pair (5-12). Since the

OTA is the only active block on the filter network (not considering the clock buffers), it is necessary to define closer to block specifications. The schematic of the OTA VHDL-AMS model is illustrated as follows:

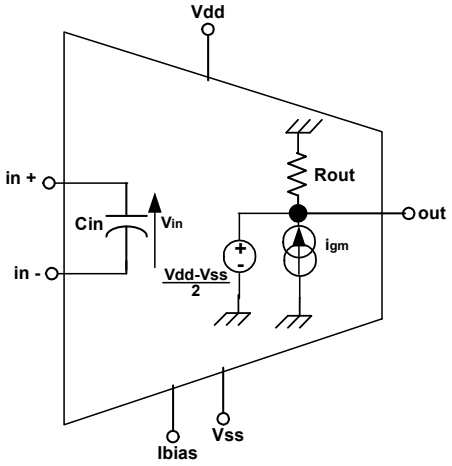


Figure 5-36 The OTA VHDL-AMS model schematic

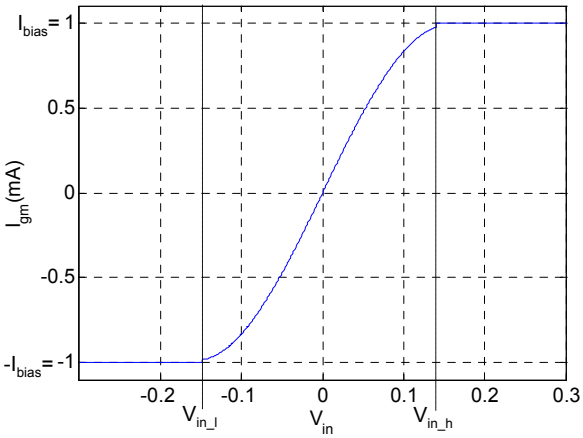


Figure 5-37 The OTA transfer curve

The OTA is basically composed of a differential input pair and a transconductance source dependent on the input differential voltage. The model is based on ([127]). The OTA open-loop gain depends on the output resistance and on the transconductance gain. Limitations on the output voltage (from Vdd and Vss) (eq) and current range (from Ibias) (eq) models the block's saturation. In addition to the model on [127], the gm(V_{in}, I_{bias}) follows a third order polynomial function (eq) as well, for non-linearity test bench. From the input ports in^+ and in^-, the differential input voltage/current are first defined:

$$I_{in} = C_{in}\frac{dV_{in}}{dt} \quad \text{where} \quad V_{in} = V_{in}^{+} - V_{in}^{-} \tag{5-65}$$

From Ibias port we define the current limit on the OTA, and the negative/positive limits on the input voltage V_{in_l}, V_{in_h} which are dependent on the defined transconductance gain and on Ibias:

$$V_{in\_l} = \frac{-I_{bias}}{gm} \qquad V_{in\_h} = \frac{I_{bias}}{gm} \tag{5-66}$$

Therefore the current source is defined as follows and is illustrated in Figure 5-37.

$$i_{gm} = \begin{cases} I_{bias} & \text{if} \quad V_{in} > V_{in\_h} \\ -I_{bias} & \text{if} \quad V_{in} < V_{in\_l} \\ V_{in} \cdot gm \cdot \left(1 - \alpha_1 \cdot V_{in} - \alpha_2 \cdot V_{in}^{\,2}\right) & \text{if} \quad V_{in} < V_{in\_h} \end{cases} \tag{5-67}$$

The output common mode is an independent voltage source:

$$Vref = \frac{Vdd - Vss}{2} \tag{5-68}$$

The dynamic output voltage is dependent on the defined thresholds (Vdd and Vss) and on the current flowing on the output resistance. Ideally, R_{out} is infinite and all the generated current flows on the next block charge:

$$V_{out} = \begin{cases} Vdd & \text{if} \quad V_{out} > Vdd \\ Vss & \text{if} \quad V_{out} < Vss \\ R_{\text{out}} \cdot \text{I}_{\text{R\_out}} & \text{if} \quad V_{in} < V_{in\_h} \end{cases} \tag{5-69}$$

The complete code is in APPENDIX E .

4.1.3 The filter block schematics and the TF validation

The sampling block follows a continuous time *IF1* filter. Since this filter is a differential structure, two sampling capacitors are connected to the filter. These capacitors are connected to the ground, which characterizes a pseudo-differential structure. The filter is also set pseudo-differential in order to implement the negative coefficients Figure 5-38. The FIR stage (Figure 5-15) is composed of eight capacitors by path (two per coefficient). The VHDL-AMS implementation is illustrated in Figure 5-38.

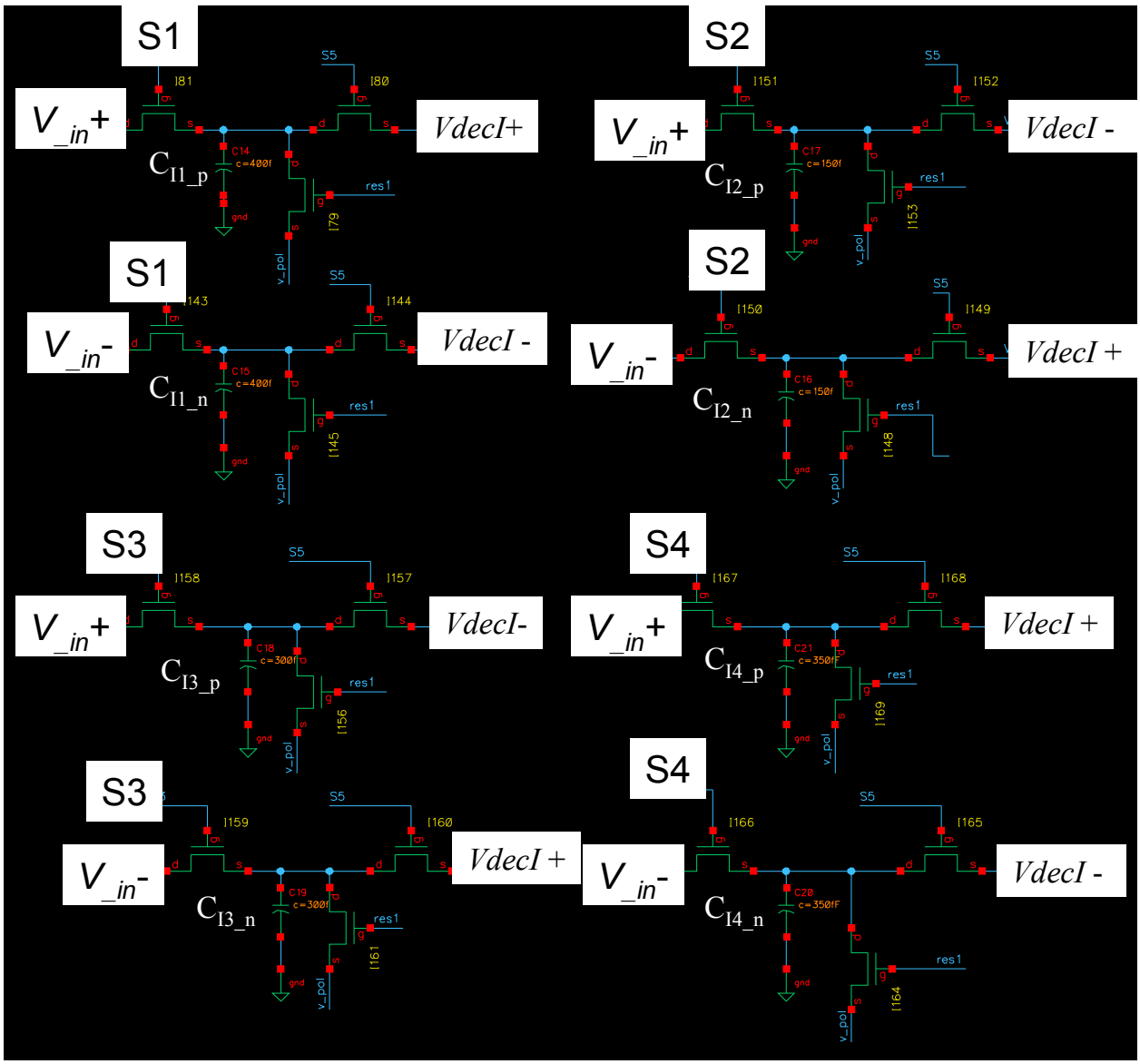


Figure 5-38 The FIR stage on the I path

To implement the negative sign of the complex filtering, the negative and positive capacitors are inverted on the decimation phase. In order to implement the IIR complex filter

(section 2.5.1), four OTA are connected to the negative and positive nodes from I and Q paths. The modeled OTA on the filter network is illustrated in Figure 5-39:

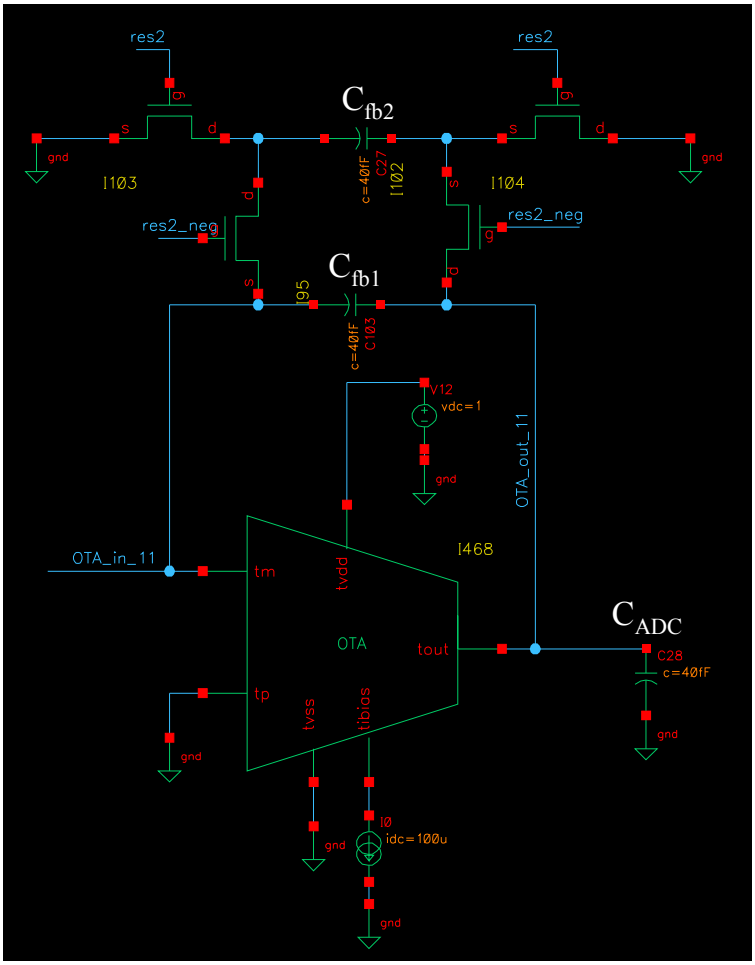


Figure 5-39 : The simulated OTA and the capacitive feedback loop

We remind the clock strategy for the clock phases S6 to S9 which defines the feedback loop for the complex IIR filter:

	OTA_1	**OTA_2**	**OTA_3**	**OTA_4**
S6	I+	I-	Q+	Q-
S7	Q+	Q-	I-	I+
S8	I-	I+	Q-	Q+
S9	Q-	Q+	I+	I-

Table 5-7 : The connection schematics on the OTAs' input

In order to verify the TF, a transient simulation is set. Different tones are summed at the filters input, and the difference between the tones inputs and outputs set the transfer function for the filter. The input signal bandwidth is the difference between the last and the first tones center frequencies. The signal is bandpass sampled, filtered and decimated. The applied sampling frequency is fs=100*MHz*. The input signal frequency varies from 2 GHz to 2.05 GHz (Figure

5-40). After BPS of the signal, the band of interest is from -50 MHz to 50 MHz. Since a decimation by four is implemented, f_{ADC}=25 MHz, the output spectrum is considered from -12.5 MHz to 12.5 MHz. Every signal from -50MHz to 50MHz will be aliased to this region. In order to avoid aliasing of a signal, which occupies a band of 50MHz, the simulation is separated in four test benches. The TF is evaluated for each region combined on the output:

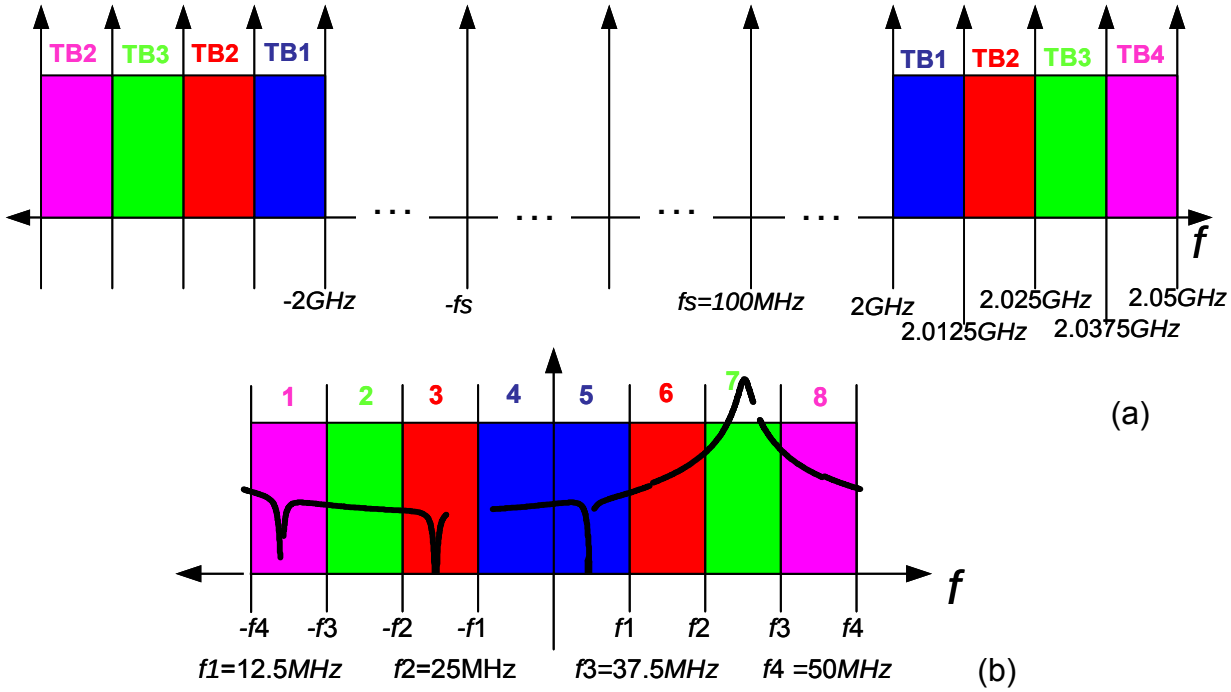


Figure 5-40 : Frequency plan for the filter validation test bench; (a) before sampling, (b) after sampling

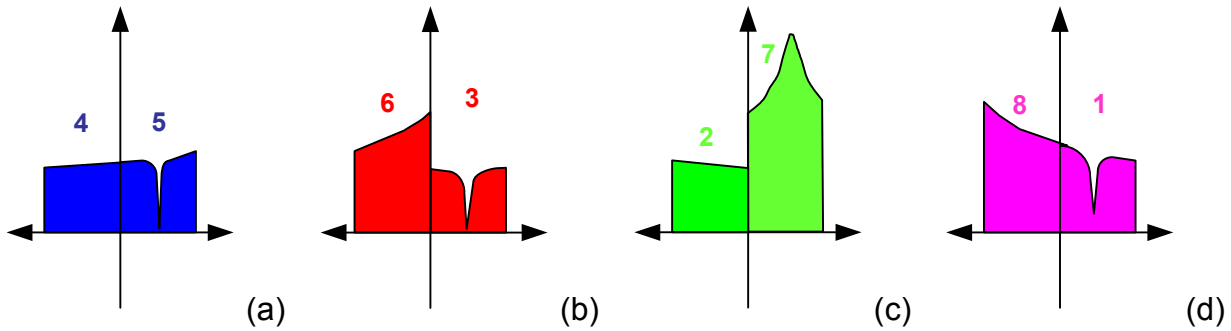


Figure 5-41 : Test benches output after decimation; (a) TB1, (b) TB2, (C) TB3, (d) TB4

The transient simulation considers a CT signal. The DT transfer function is obtained by applying a discrete *Fast Fourier Transform* (FFT) which sampling ratio is f_{ADC}=25MHz. Two real signals represent the output. For illustration, we consider the third test bench (Figure 5-41 (c)) To verify the complex TF, I(f)+jQ(f) is plotted:

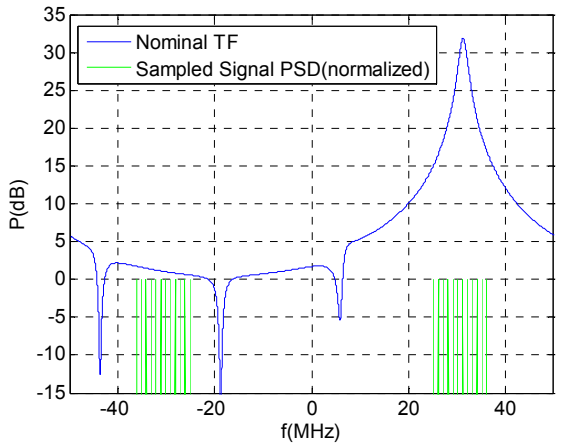


Figure 5-42 : Sampled signal for TB3 normalized PSD and the filter theoretical TF

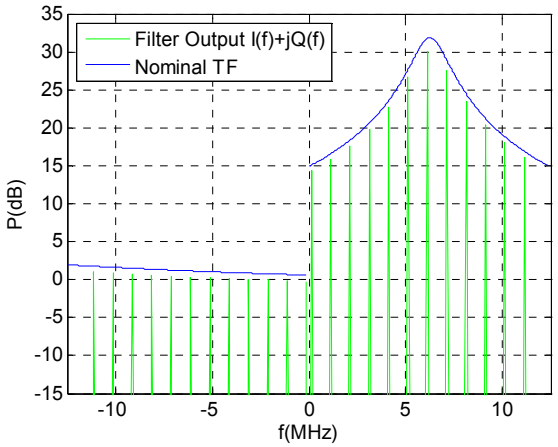


Figure 5-43 : Output PSD for TB3 and the theoretical TF

As observed, the decimated and filtered signal follows the theoretical TF. The reference TF is the one considering the unit capacitance of C_u=50fF, therefore the capacitances of Table 5-4. The frequency response is illustrated in Figure 5-24 and Figure 5-25. In an ideal case, with no parasitic capacitances and a linear OTA, the following frequency response is obtained :

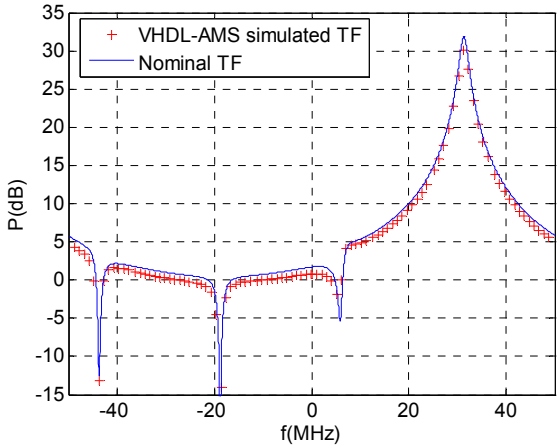


Figure 5-44 : Sampled signal normalized PSD and the filter theoretical TF

The filter TF is therefore validated through VHDL-AMS simulation. We observe the agreement of the simulated and the analytical nominal TFs. In the next sections, the parameters inside VHDL-AMS model will be changed in order to take into account the influence of blocks imperfections on the filtering TF.

4.2 The parasitic capacitances impact on the filter TF

In section 4.1.2 the VHDL-AMS models have been described. One of the objectives of the behavioral modeling is to verify how sensitive to parasitic capacitances the filtering TF is. Consider the filter lowest capacitor on the FIR stage set as Cl . The capacitor values used in the test are summarized in Table 5-4, the lowest capacitance of the FIR stage is Cl=150fF. From Figure 5-35, the capacitors C_{gs} and C_{gd} (defined as Cp) have been set from Cp/Cl=3.33% to Cp/Cl=20%. The applied test bench is summarized in Figure 5-40. The filter TF is obtained by interpolation of the output data and analyzed on the center frequency and on the filter notches. The frequency limits fl and fh are defined considering the center frequency or the notches

frequencies and the bandwidth occupied by a BT-LE modulated signal around these reference frequencies.

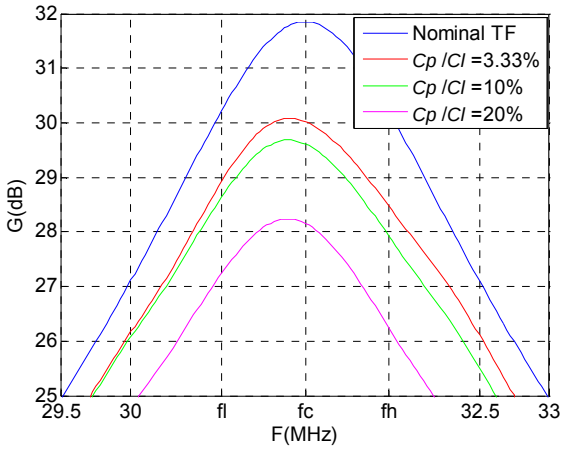


Figure 5-45 : Effect of the parasitic capacitances around the filter center frequency

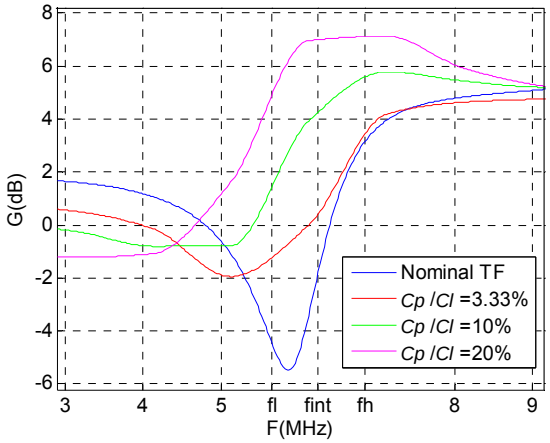


Figure 5-46 : Effect of the parasitic capacitances around the interferer @ fs/16

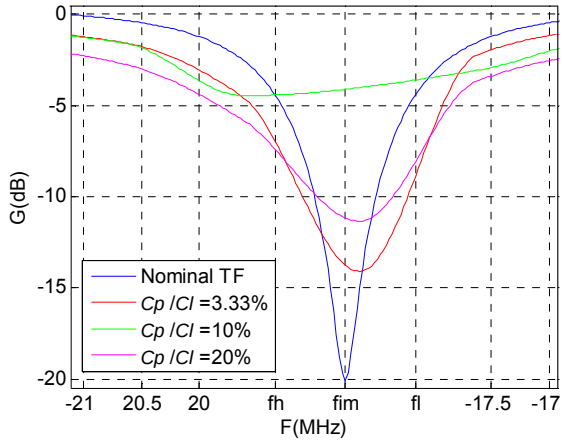


Figure 5-47 : Effect of the parasitic capacitances around the image frequency fim= -fs/4+fs/16

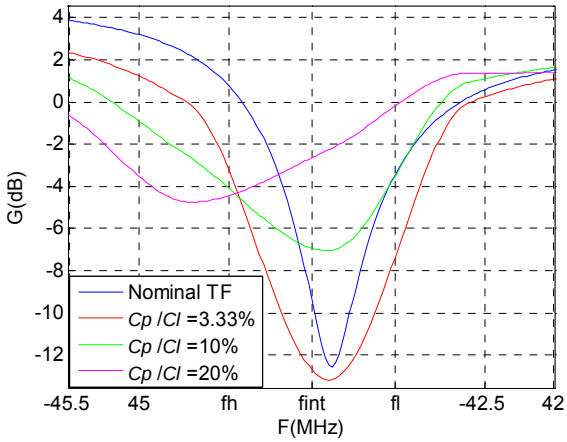


Figure 5-48 : Effect of the parasitic capacitances around the interferer @ -fs/2 +fs/16

Table 5-8 summarizes the performance degradation and the rejection for the aliasing interferers and the image. The rejection is defined as the ratio between the lowest gain on Figure 5-45 (fh or fl) and the highest gain on Figure 5-46, Figure 5-47 and Figure 5-48 (fh or fl).

	Δint @ fs/16 (dB)	Δint @ -fs/2+-fs/16 (dB)	Δim (dB)
Nominal	27	29.5	34.6
Cp/Cl=3.33%	25	31.7	35.5
Cp/Cl =10%	22.3	31.5	31.5
Cp/Cl =20%	19.1	26.4	33.7

Table 5-8 : The filter performance in presence of parasitic capacitances

The image rejection specification is respected in all cases. The worst observed performance is the interferer rejection @ fs/16 of Δint =19dB. Considering the highest switch size, which is the sampling switch considering the highest frequency constraint, the Cp/Cl ratio can be higher than 20%. On the other hand, after sampling, slower time constants can be set. This allows reducing significantly the switch size (increasing R_{ds}) without impacting the needed

cut-off frequency. This switch size reduction enables to reduce the parasitic capacitances along the filter network. The switches are therefore separated in three types: Sampling switch Ss, averaging FIR stage switch S_{FIR} and reset switches S_{res}. The reference cut-off frequencies and the filter capacitances lead to calculate the compatible R_{ds}. From the ST CMOS 65nm technology model, we consider the simulated C_{gs} and C_{ds} given the required R_{ds} and the defined common mode Vcm. On the following test bench the switches are set as follows:

Ss : Cp/Cl =40% S_{FIR} : Cp/Cl =6.7% S_{res} : Cp/Cl =8%

The filter performance is summarized below:

Δint @ fs/16 (dB)	Δint @ -fs/2+-fs/16 (dB)	Δim (dB)
23.5	32.1	35.5

Table 5-9 : The filter performance on the optimized test bench

The parasitic capacitance degrades mostly the rejection for the interferer @ fs/16 and becomes a critical point since the filter performance is just 3dB over the specifications. On the other hand, further switch sizing optimization will reduce even further the parasitic capacitances along the filter network.

4.3 Timing Management - The Clock Tree and RC Time Constants

Very high center frequencies are presented at the input of the sampling system. The time constant fixed by the sampling switch and the sampling capacitor fixes the system cut-off frequency. In the VHDL-AMS behavioral model, the switch contains non-zero R_{on} and the parasitic capacitance is inversely proportional to R_{on}. Despite the noise constraints, the choice of the capacitor will also set the size of the switch and therefore, the amount of parasitic capacitances on the context. Knowing Cs=800fF the highest allowed R_{on} is set to R_{on}=40Ω in order to have fc ≈ 5GHz. This frequency permits to have very few losses on the S/H low-pass filtering (eq 12 of CHAPTER 2), but still does not need to respect the $5\sigma<1/f_H$ defined for Nyquist sampling (section 2.2.3 of CHAPTER 2).

On the clock tree side, the clock phases are set in Figure 5-4 and Figure 5-17. The clock tree model implemented in VHDL considers the sampling clock as reference and the clock phases are generated from three basic blocks: Boolean logic, delay cells and counters. The reference sampling frequency is fs=100MHz. Considering the duty cycle of 50%, the clock is at "1" or "0" during 5ns. When analyzing the clock strategy defined in section of Figure 5-4, the most critical phase is at the decimation S5 and the reset Sres stages. On the interval of 5ns, the capacitors are charge shared on the decimation and the reset phase must be completed before S1 goes to "1" for the next set of FIR samples (Figure 5-49).

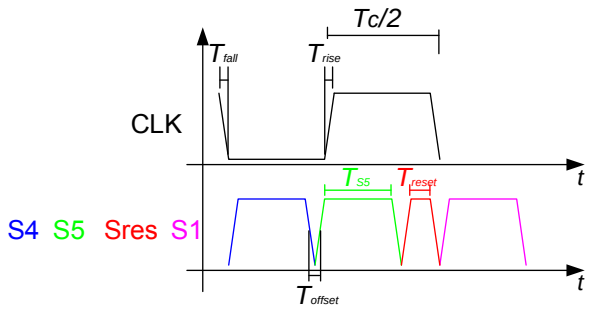


Figure 5-49 : The clock strategy and the constraining time references

Once the filter capacitors are charge shared with the feedback capacitors, the OTA transfers the charge to the output. The decimated frequency is f_{ADC}=25MHz. On the implementation side, the power consumption is proportional to the G·BW product; therefore, the power consumption depends on the required gain and on T_{S5}. The system gain depends on T_{S5}. Table 5-10 summarizes the filter gain on the pass band for different configurations of T_{S5} and gm_{OTA}. First S5=2ns, the open-loop gain is kept A0=100, which means that R_{out} also changes for the different test benches. Then S5=3ns is set, and we observe an increase of the gain for the same gm_{OTA} mainly for gm_{OTA}=1mS.

	S5=2ns	S5=3ns
Nominal	29 dB	29dB
gm_{OTA} = 1mS	25.4 dB	26.6 dB
gm_{OTA} = 2mS	27 dB	27.7 dB
gm_{OTA} = 5mS	28 dB	28.2 dB

Table 5-10 : The filter gain for different gm_{OTA} and $S5$

Since T_{S5} is a constraining part for the OTA stage, a new clock strategy can be envisaged based on double sampling. This means that while one FIR stage capacitors have their charge transferred to the feedback capacitors, another FIR stages is applied on the input to get the next N samples. S5 can be therefore expanded to $1/f_{ADC}$ strongly relaxing gm_{OTA} G·BW constraints. Since the double network is completely passive, no additional power consumption is expected while applying double sampling. On the other hand, block surface is doubled, since most of the surface is defined by the filter capacitors. Finally, we decided to keep the single structure while using the gm_{OTA}=1mS and T_{S5}=4ns which relaxes the OTA while the clock tree rising and falling edges are optimize for that goal.

4.4 OTA impact on the filter TF

One of the objectives in this section is to verify the feedback loop on the filter IIR stage on VHDL-AMS environment. The feedback network is defined on Figure 5-39. We apply the capacitances derived in Table 5-4 and finite gains of A0=50, 100, 150. The simulated results are

compared with the nominal transfer function of (5-36) and (5-37) while considering the effects of finite gain of (5-45) and (5-46):

The resulting closed-loop gain and feedback coefficient are compared with:

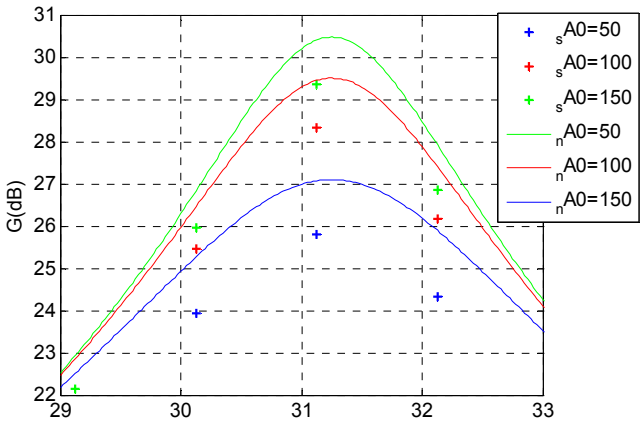


Figure 5-50 : Frequency response, simulated (s) and the nominal (n) for different A0;

When the results from Figure 5-50 are compared with the nominal frequency response, 1dB gain loss is observed between the theoretical and simulated TF. This effect is due to addition parasitic capacitances on the analysis.

4.5 Intermodulation product analysis IIP3 validation

In this section we analyze the filter output spectrum when the switch R_{ds} follows a non-linear behavior. In this test bench the OTA is considered linear and the filter *Input Referred Third Order Intercept Point* IIP3 specified in CHAPTER 4 is to be verified. As it was defined in section 4.2, the filtering network is separated in three types of switches: sampling switch Ss, averaging FIR stage switch S_{FIR} and reset switches S_{re}. We remind the R_{eq} model defined in (5-60) and the voltage transfer function defined in (5-61). The second order polynomial on the R_{eq} lead to a third order polynomial on Vcm. R_{eq} has a nominal value on $V_{\_in}$=0. The non-linear coefficients α_1 and α_2 were set considering the technology curves. The varying resistance will have two different impacts on the filter transfer function. On the sampling phase, the R_SC_S block presents the following TF:

$$\frac{V_S}{V_{\_in}} = \frac{1}{1+sR_SC_S} \tag{5-70}$$

which means that the sampler cut-off frequency, and therefore the gain, varies with the input voltage. On the filter stage, the charge sharing requires a certain time constant to establish, dependent on R_{FIR} and R_{re}:

$$V_{out} = \left(1 - e^{-t/(R_{FIR} \cdot C_{FIR})}\right) V_{balance} \tag{5-71}$$

The error between V_{out} and$V_{balance}$ is simply a loss when R_{FIR} and C_{FIR} are constant, but in this case R_{FIR} varies over time and is dependent on the input voltage, therefore, it generates non-linearity. Both sources of non-linearity come from a varying resistance. The objective for these test benches is to find the equivalent *Third Order Intermodulation Product* (IM3) for the entire filter

network. Two tones interferer Int at 3MHz and 6MHz away from the signal of interest are applied. The signal of interest is placed at the filter center frequency, fc=2031,25MHz. The applied sampling frequency is fs=100MHz, therefore, after sampling, the interferers are placed at f_{Int1}=34,25MHz and f_{int1}=37,25MHz. After decimation, the interferers are placed at 9,25MHz and 12,25MHz, and the third order intermodulation product IM3 is placed at 6,25MHz. From the intermodulation product, the equivalent A_3 is found, and from the last we derive the IIP3 (equations 22 and 23 CHAPTER 3):

$$\frac{im3_{RMS}\cdot\sqrt{2}}{Int_1^{\,2}\cdot Int_2}\cdot\frac{4}{3}=\alpha_3 \tag{5-72}$$

$$IIP3\left(V^2\right)=\left(\frac{4}{6}\left|\frac{Gv}{\alpha_3}\right|\right) \tag{5-73}$$

For the required SNDR it is the gain for the signal of interest which has to be taken into account (CHAPITRE 4) for Gv. In order to defined the linear gain Gv, the closed-loop gain is derived from Figure 5-50 @ A0=100. The following table summarizes the equivalent IIP3 simulated for different configurations of α_1 and α_2

	α_1/R_{ds}	α_2/R_{ds}	Int (dBmW(50Ω))	IM3 (dBmW(50Ω))	IIP3 (dBmW(50Ω))
TB1	-7	20	-40	-63.75	23
TB2	-10	30	-40	-36.9	9.7
TB3	-12	40	-40	-28.3	5.4

Table 5-11 : The test benches definition for the intermodulation product analysis through VHDL-AMS

In any case from Table 5-11 the derived IIP3 for the filtering stage is largely above the required on (table 1-15 of CHAPTER 4). The results from Table 5-11 are technology independent. In order to fit the application with the technology, we have to define if the values from the technology for α_1 and α_2 are in agreement with the values α_1 and α_2 from Table 5-11 that leads to compliant IIP3. Considering the ST NMOS transistor with 65nm technology, we applied parametrical simulation in order to derive the R_{eq} vs $(1-V_{gcm})$ for the different applied resistances (R_S R_{FIR} and R_{res}) (Figure 5-51). The derived non-linear coefficients for the simulated switch was α_1/R_{ds}=0.2 and α_2/R_{ds}=3.05 considering R_{ds}=13.44Ω at Vcm=0.2V.

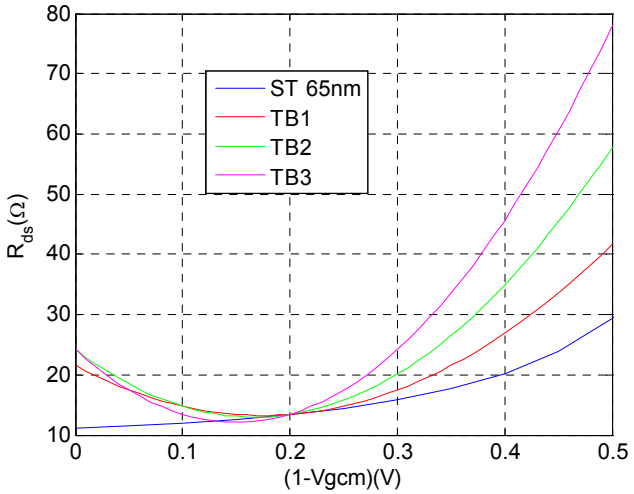


Figure 5-51 : R_{ds} vs (1-Vgcm) for R_{ds}=13.44Ω @ Vcm=0.2V

In conclusion, the applied technology is greatly sufficient in terms of linearity, considering the applied Vcm=0.2 and only a single NMOS transistor used as switch. The techniques of clock boosting and dummy transistors [128] are proven to be unnecessary in our application, considering the low dynamic range of the input signal on the sampling and the IIP3 distribution on the system level design of CHAPTER 4 – table 1-15. The block is being developed in our laboratory and a consistent IIP3 is found considering the derived α_1 and α_2 for the technology and the VDHL-AMS simulation.

5 Conclusion

In this chapter, the proposed complex IIR filter, which is used between the BPS process and the ADC, is studied in detail. The theory of the DT filtering is presented. The filter topologies get more complicated step by step, from FIR filters to IIR filters and finally complex IIR filters. The presented theory leads to the definition of the filter coefficients for the proposed filter in CHAPTER 4. The transfer function is analyzed and the frequency response is validated regarding the required system level specifications. The chosen filter present a 4^{th} order IIR complex filter, with feedback coefficient of 0,8.

Although it is mostly implemented in the digital domain, the analog implementation of such filtering functions is also possible. The basic MAC operation is implemented by the charge sharing phenomenon. Each DT filter topology can be implemented in the analog domain by applying switched capacitor blocks. The combination of the analog implementations for the different DT filter topologies lead to propose a block implementation of the DT complex IIR filter.

A list of possible block imperfections is defined. These imperfections include: a varying filter group delay inside the band of interest, finite resolution on the coefficient values, dispersion on the coefficient values, thermal noise, parasitic capacitances, clock tree constraints (gain bandwidth product, RC bandwidths), OTA finite gain and non-linearity.

In order to know the impact on the required frequency response of each of these imperfections, analytical developments and behavioral VHDL-AMS simulations were carried out. On the VHDL-AMS development, the theoretical frequency response is found for a nominal case, which calibrates the simulation environment, out of the imperfections are added and the resulting performances evaluated.

General conclusions over the imperfections are the following:

- **Varying group delay:** The correct filter bandwidth/selectivity ratio is known applying a feedback coefficient of β=0.8. The distortions coming from non-linear phase have no major impact on the required SNDR.

- **Finite resolution:** From ST CMOS 65nm data, the chosen unit capacitance is Cu=50fF. The coefficients generated from Cu=50fF permits not only very performing match with theoretical TF but also to reduce capacitor mismatches.

- **Coefficients dispersion:** Compared to the required filter performances of CHAPTER 4, the filter is still compliant with the proposed architecture and standards up to a standard deviation of 3% on the capacitor mismatches and 30% deviation on the OTA open-loop gain. From ST CMOS 65nm data and Cu=50fF, this mismatch is under 0.2%. Up to 5% and 5º gain and phase mismatches are allowed and the filter is still compliant with the architecture and the standards.

- **Thermal noise:** From theoretical analysis, an equivalent NF for the sampler + filter of 15dB over the sampler only has been found, which leads to the need of an amplification stage between the sampler capacitor and the filter capacitors. The analytical development is validated through block noise transient simulation with 2.3dB difference.

- **Parasitic capacitances:** The filter can tolerate up to Cp/C_I = 40% on the input switches and Cp/C_I=10% for the rest of the switches respecting the required rejections for image and aliasing interferers, which are easily respected for the applied switch sizes.

- **Clock tree constraints:** The charge transfer time on the OTA input is very constraining regarding its G·BW product. Considering a gm_{OTA}=1mS and A0=100, 2,4dB losses from the nominal gain are observed on the simulation.

- **OTA finite gain:** The OTA finite gain impacts not only the closed-loop gain but also the feedback coefficient. We have to keep in mind that, regarding the power consumption, the smaller the OTA gain, the better. A good trade-off is observed applying A0=100.

- **Non-linearity:** The result IIP3 is simulated for the sampler + filter block, considering only the non-linearity on the switches. A parametric simulation shows the impact of the non-linear coefficients α_1 and α_2 for the R_{ds} model polynomial. From Table 5-11 we observe that for α_1/R_{ds}=-12 and α_2/R_{ds}=40 the filter is still largely linear, considering this test bench worse than compared to the ST 65nm simulated α_1 and α_2.

  The last impairments on block to be analyzed are the impact of clock jitter and PLL/DLL phase noise on the BPS process. Analytical development and numerical method are the tools to carry out this study. The next chapter is dedicated to present this critical point.

APPENDIX D : THE SWITCH VHDL-AMS CODE

```
--
-- ADVance MS model for sampler_lib sampler_stellarv4_ssimple adms_vhdlams
--
LIBRARY DISCIPLINES;
USE DISCIPLINES.ELECTROMAGNETIC_SYSTEM.ALL;

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.MATH_REAL.ALL;
USE WORK.ALL;


ENTITY sampler_stellarv4_ssimple_adms_vhdlams IS
      GENERIC (r_on : REAL :=20.0;
             r_off : REAL :=100.0e6;
             alfa1 : REAL := 100.0;
             alfa2  : REAL  :=200.0;
             c_gs : REAL :=1.0e-15;
             s1 : positive :=111;
             s2 : positive :=333
      );
      PORT (TERMINAL g, s, d : ELECTRICAL
      );
END;

ARCHITECTURE adms_vhdlams OF sampler_stellarv4_ssimple_adms_vhdlams IS
QUANTITY vg ACROSS g TO ELECTRICAL_GROUND;
QUANTITY vd ACROSS d TO ELECTRICAL_GROUND;
QUANTITY vs ACROSS d TO ELECTRICAL_GROUND;


QUANTITY vds ACROSS ids THROUGH d TO s;
QUANTITY vgs ACROSS igs THROUGH g TO s;
QUANTITY vgd ACROSS igd THROUGH g TO d;

QUANTITY rds : REAL := 10.0e6;
QUANTITY vcm : REAL := 0.0 ;

--CONSTANT cgs : REAL := 1.0e-15;
--CONSTANT cgd : REAL := 1.0e-15;

signal S_NOISE : real :=0.0;


BEGIN

process is
variable X1,X2,X: REAL := 0.0;
variable SD1: POSITIVE := s1;
variable SD2: POSITIVE := s2;
begin
UNIFORM(SD1, SD2, X1); -- uniform gives a value 0<x<1
UNIFORM(SD1, SD2, X2); -- defined in ieee.math_real
X:=(((4.0*1.38e-23*300.0*rds/(2.0*40.0e-
12)))**0.5)*COS(MATH_2_PI*X1)*SQRT(-2.0*LOG(X2));
S_NOISE<=X;
wait for 40.0e-12;
end process;

      IF (vg>0.5)
```

```
            USE rds==r_on;
            ELSE rds==r_off;
      END USE;

vcm==(vd+vs)/2.0;
vds==((rds-alfa1*(vcm)-alfa2*(vcm)**2)+alfa1*(1.0-(vg-vcm))+alfa2*(1.0-(vg-
vcm))**2)*ids ;-- +S_NOISE'ramp(1.0e-15,1.0e-15);
igs==c_gs*vgs'DOT;
igd==c_gs*vgd'DOT;

END;
```

APPENDIX E : THE OTA VHDL-AMS CODE

```
 --
  -- ADVance MS model for sampler_lib OTA adms_vhdlams
--
LIBRARY DISCIPLINES;
USE DISCIPLINES.ELECTROMAGNETIC_SYSTEM.ALL;

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.MATH_REAL.ALL;
USE WORK.ALL;

ENTITY OTA_adms_vhdlams IS
      GENERIC (gm0 :real :=100.0e-6; --transconductance
               c_in  :real :=300.0e-15; --input capacitance
              r_out : real :=10.0e+3;  --output resistor
              alfa1 :real :=0.0; --transconductance
              alfa2 :real :=0.0 --transconductance
              );
      PORT (terminal Tp, Tm, Tout, Tibias, Tvdd, Tvss: electrical
      );
END;


ARCHITECTURE adms_vhdlams OF OTA_adms_vhdlams IS
---***external quantities***--
quantity v_in across i_in through Tp to Tm ; --input differential voltage
quantity v_out across i_r_out through Tout to electrical_ground ; --input
differential voltage


--high/low power supply voltage
quantity vdd across Tvdd to electrical_ground;
quantity vss across Tvss to electrical_ground;

--bias current
quantity Vibias across ibias through electrical_ground to Tibias;

---***internal quantities***---
-- power middle point/low/high input saturation voltage
quantity vref, vinl, vinh: real:=0.3;

--transconductance current source
quantity igm through electrical_ground to Tout;



BEGIN
-- -***input/output stage***---
i_in==c_in*v_in'DOT;


---***transfer stage***---
Vibias==ibias*10.0;

vref==(vdd+vss)/2.0;
vinl==-ibias/gm0;
vinh==ibias/gm0;
```

```
---***voltage and current limitations***---
if v_in'above(vinh) use igm==ibias;
elsif not v_in'above(vinl) use igm==-ibias;
else
igm==v_in*gm0*(1.0-alfa1*v_in-alfa2*v_in**2); end use;

-----***voltage and current limitations***---
if v_out'above(vdd) use v_out==vdd;
elsif not v_out'above(vss) use v_out==vss;
else v_out==r_out*i_r_out+vref; end use;


END ARCHITECTURE adms_vhdlams;
```

APPENDIX F : ANALYTICAL DEVELOPMENT FOR THE FILTER OUTPUT NOISE POWER SPECTRAL DENSITY

We remind the FIR stage noise schematic from section 3.5.1:

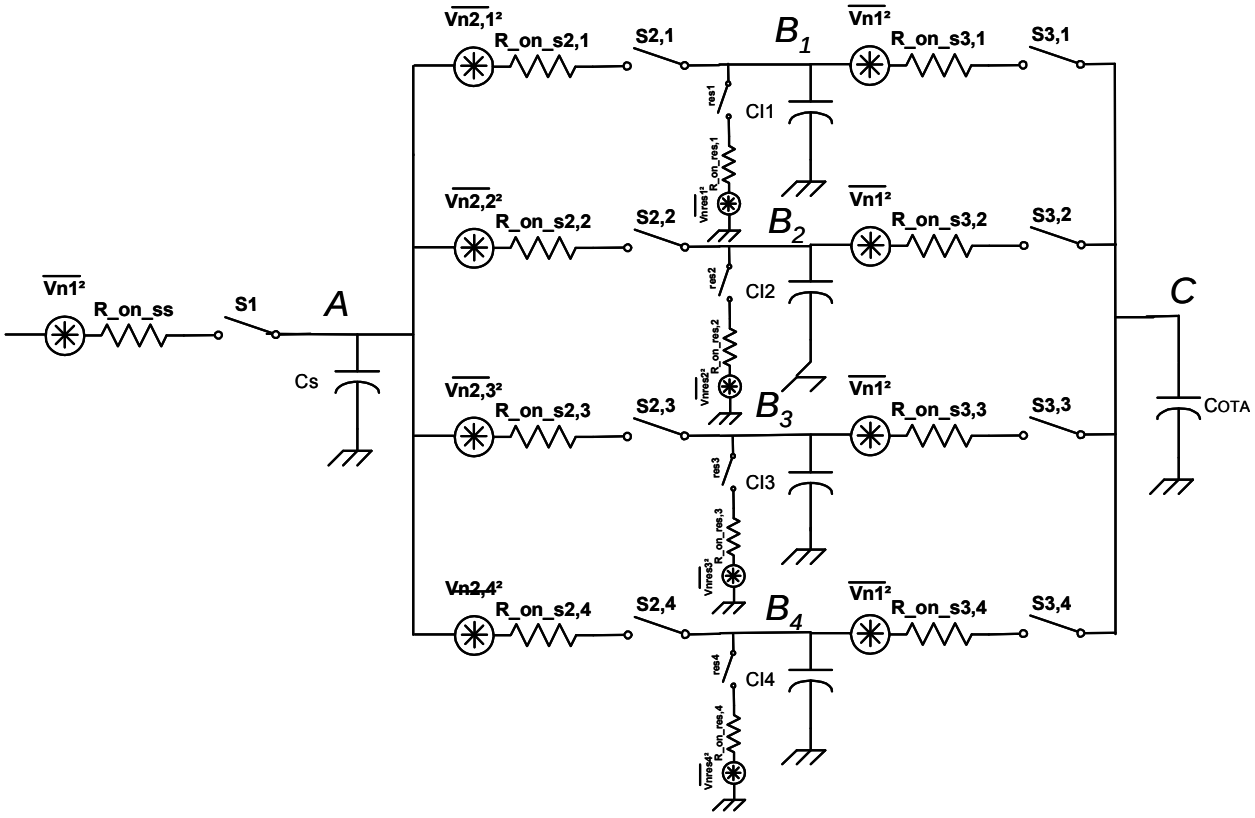


Figure 5-52 Equivalent noise schematic for the FIR stage on the I+ path

We consider the first switch on the filter that, on *S1*, stores *KT/Cs* noise in *Cs*, the voltage between *Cs* to *CIn* is defined in (5-31). The noise is cumulated 4 times in power (the four FIR filter samples) and summed in power, the power transfer function of (5-31) is considered, on the decimation stage (5-32), an additional capacitor is taken into account, considering the OTA access capacitance:

$$\overline{Vn1^2}_{,A} = \frac{kT}{Cs}\left(V^2\right) \tag{5-74}$$

$$\overline{Vn1^2}_{,Bk} = \overline{Vn1^2}_{,A} \cdot \left(\frac{Cs}{\left(Cs + C_{In} + C_{Qn}\right)}\right)^2 \tag{5-75}$$

$$\overline{Vn1^2}_{,C} = \sum_k \left[\overline{Vn1^2}_{,Bk} \cdot \frac{C_{Ik}^{\ 2}}{C_{TOT}^{\ 2}}\right] \tag{5-76}$$

$$C_{TOT} = \sum_k C_{Ik} + C_{OTA} \tag{5-77}$$

Now, from Figure 5-33, we analyze the noise generated by the FIR switches *S2,n. The Kirchhoff Current Law* (KCL) is applied to evaluate the noise power on *Bk* generated by *S2,kI*:

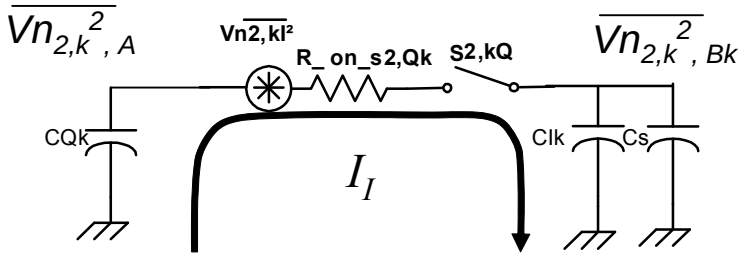


Figure 5-53 The noise generated on *R2,k*

$$-\frac{I_I}{s\left(Cs+C_{Qk}\right)}+Vn2,k-I_I\cdot R_{onS2,k}=\frac{I_I}{sC_{Ik}}=Vn2,k_{Bk1} \tag{5-78}$$

$$Vn2,k,_{Bk1}=Vn2,k\cdot\frac{\dfrac{Cs+C_{Qk}}{Cs+C_{Qn}+C_{Ik}}}{1+s\dfrac{R_{onS2,1I}\cdot C_{Ik}\cdot\left(Cs+C_{Qk}\right)}{Cs+C_{Qk}+C_{Ik}}} \tag{5-79}$$

The generated noise is *4KTR_on_s2,k* which passes by the first order transfer function. The equivalent DC gain and cut-off frequencies are:

$$G=\frac{Cs+C_{Qk}}{Cs+C_{Qk}+C_{Ik}} \tag{5-80}$$

$$fc=\frac{1}{2\pi}\cdot\frac{1}{\dfrac{R_{onS2,1I}\cdot C_{Ik}\cdot\left(Cs+C_{Qk}\right)}{Cs+C_{Qk}+C_{Ik}}} \tag{5-81}$$

The total noise is given by:

$$\overline{Vn2,k^2}_{,Bk_1}=4KTR_{onS2,kI}\cdot G^2\cdot\frac{\pi}{2}fc=KT\cdot\frac{Cs+C_{Qk}}{C_{Ik}}\cdot\frac{1}{Cs+C_{Ik}+C_{Qk}} \tag{5-82}$$

Since the switch of the opposite phase is also connected to *CIk* on the first charge sharing, it is also considered this noise on *Bk* :

$$\overline{Vn2,k^2}_{,Bk_2}=4KTR_{onS2,kQ}\cdot G^2\cdot\frac{\pi}{2}fc=KT\cdot\frac{C_{Qk}}{Cs+C_{Ik}}\cdot\frac{1}{Cs+C_{Ik}+C_{Qk}} \tag{5-83}$$

$$\overline{Vn2,n^2}_{,Bn}=KT\cdot\frac{1}{Cs+C_{In}+C_{Qn}}\cdot\left(\frac{Cs+C_{Qn}}{C_{In}}+\frac{C_{Qn}}{Cs+C_{In}}\right) \tag{5-84}$$

The noise $S_{B,k}$ is cumulated four times and charge shared on the output:

$$\overline{Vn2^2}_{,C}=\sum_k\left[\overline{Vn2,k^2}_{,Bk}\cdot\frac{C_{Ik}^{\ 2}}{C_{TOT}^{\ 2}}\right] \tag{5-85}$$

On the reset step, only the reset switch is connected and the noise is integrated on *Cn*:

$$\overline{Vn\_res^2}_{,C}=\frac{KT}{C_{TOT}}\sum_{nk}CIk\left(V^2\right) \tag{5-86}$$

On the output stage, *S3,k* and *S,OTA* will generate noise as well, the Kirchhoff Current law is calculated on the output level as it was for Figure 5-53:

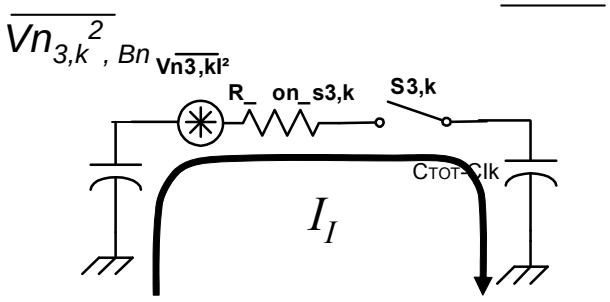


Figure 5-54 The noise generated on *R3,k*

As it was derived for (5-84), the output noise power from *S3,k* is given by:

$$\overline{Vn3^2}_{,C} = KT \cdot \frac{1}{C_{TOT}} \cdot \sum_{k} \left(\frac{C_{Ik}}{C_{TOT} + C_{Ink}} \right) \tag{5-87}$$

The proposed architecture is been developed in an subsequent project which down to the silicon level, were the expectation on the measurement results is very promising considering the results presented in this thesis. Simulation results on post layout level for the FIR stage from the proposed DT filter have already confirmed the parametrical simulation presented in chapter 5 and current developments are concentrated on the OTA IIR filter. Further studies potentially interesting consist on analyzing different techniques on the IF1 filter level. Finally, the specifications on the IF1 filter are moderate, even relaxed, in order to present an on-chip solution, structures based on LC resonators could be analyzed. On the DT filter level, another interesting application is the attempt to apply more selective filter (such a complex IIR plus Sinc² filter) in order to suppress IF1 stage. This technique will notably lead to more complex DT filter but the advantages of a high under-sampling factor and the possibility to apply IIR filters on low-IF architectures are kept.

Chapter 6 : The Phase Noise Specifications on the Proposed Architecture

1 Introduction

The BPS architecture proposed in Chapter 4 enables to relax constraints on the frequency synthesis by reducing oscillator frequency. In order to conclude about the benefits in terms of power consumption, phase noise specifications have to be evaluated in this context.

Yet, some aspects of phase noise in BPS are not completely closed. In particular the impact on arbitrary jitter in the BPS process is to be analyzed in depth. It is important to know if BPS represents or not an increase on the jitter specifications constraints, which would reduce the interest of decreasing the frequency synthesis. The classical approach to derive the phase noise specifications has to be reconsidered in the framework of the BPS. It is particularly adapted to the mixing process or to Nyquist rate sampling process.

In order to cover this subject in our architecture, a numerical method able to evaluate the BPS *Signal to Jitter Distortion Ratio* (SDjR) within a given band of interest (the bandwidth around the IF, result of down-conversion on the BPS process), is developed in this Chapter. The proposed method allows applying arbitrary jitter and signal inputs (ex. random *Gaussian Frequency Shift Keying* (GFSK) modulated data and PLL based jitter). An analytical approach is developed using a simple test bench case where the jitter distribution is uncorrelated in order to validate the method.

On the following, a GFSK modulated signal is used as input and different jitter models are applied. The PLL and DLL phase noise behaviors are studied, in order to have precise jitter models containing realistic frequency synthesis circuit design issues.

The system level specification methodology presented in Chapter 3 is applied on the proposed BPS architecture of Chapter 4. For the sampling block level, the constraints are divided between the different sources of degradation on the SNDR. Hence an SDjR requirement is derived in this context and it is translated into phase noise specifications thanks to the analysis developed in this Chapter for BT-LE and IEEE802.15.4 (Chapter 3).

Using the numerical method we define the phase noise specifications and the results are compared to the state of the art of Chapter 2 in order to conclude about the possibilities to save power while applying low sampling and mixing frequencies.

2 Context - The Phase Noise Impact in Classical Architectures

In a system level analysis, in order to correctly define phase noise specifications in a receiver, the LO PSD is no more considered as being a single Dirac on the given frequency f_{LO} but a signal containing a certain amount of phase noise which follow a $1/f^2$ behavior and a flat noise floor (Figure 3-6). Phase noise of LO is derived in [129] showing its dependency to the power consumption of such blocks.

This section presents the approach to define phase noise specifications when classical processes are applied, i.e. mixing and Nyquist rate or over-sampling. On the following, we explain why such approach needs to be improved in order to specify accurate phase noise specifications for BPS systems. Therefore, we define some points to enhance the analysis.

2.1 The Phase Noise Consideration in the Mixing Operation

A classical approach to define phase noise specifications from system level analysis can be found in [97]. In frequency domain, a mixing process is a convolution between the mixer in frequency domain M(f), which is around f_{LO} and the signal of interest $S_{RF}(f)$, around f_0 (Figure 3-6 (a)). The mixed signals contain a portion which is correlated to the signal of interest and distortion coming from mixed phase noise. The IF (Figure 3-6 (b)) to consider f_{IF} is either $f_{IF} = f_0 - f_{LO}$ or $f_{IF} = f_0 + f_{LO}$

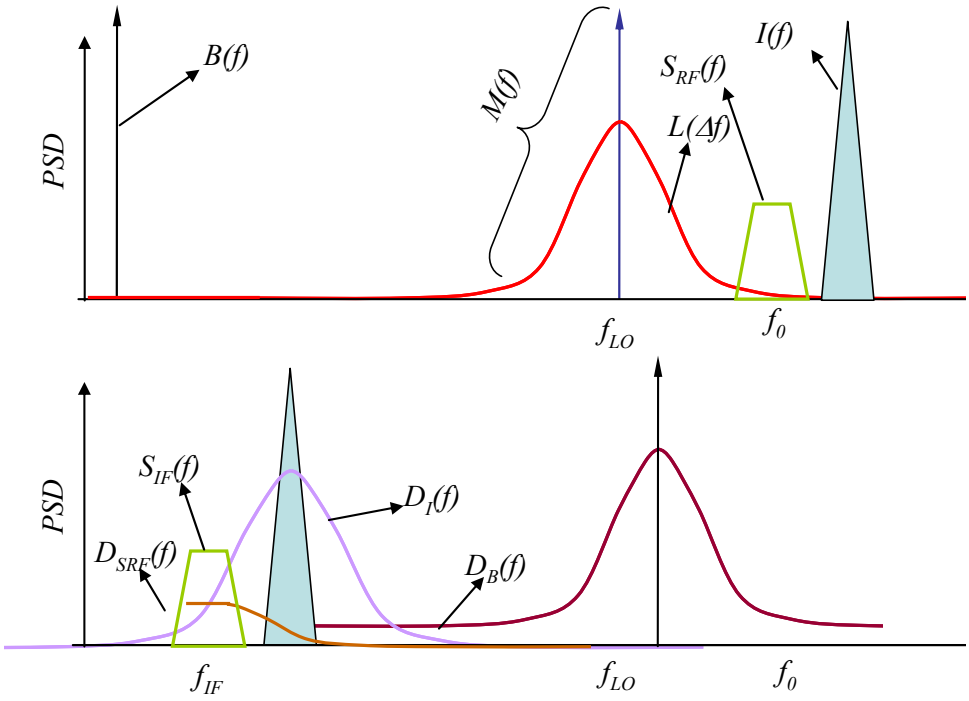


Figure 6-1 : The mixing operation in the presence of phase noise

Three distinguished sources of error appear in the mixing process in presence of phase noise (Figure 6-1 (b)). The phase noise from M(f), which is defined as L(Δf), is convoluted with

$S_{RF}(f)$ and generates a distortion around f_{IF}, defined as $D_{SRF}(f)$, which is due to the signal of interest itself. The second distortion is the convolution product between an interferer I(f) and L(Δf), defined as $D_I(f)$. It falls within the band of interest f_{IF}. $D_I(f)$ is often the strongest distortion signal and defines the oscillator phase noise specifications. A third phenomenon observed is the convolution product between an out-of-band blocker B(f), considered as a cosine wave signal, and the white phase noise floor of L(Δf) far from f_{LO}, defined as $D_B(f)$.

Let's introduce the signal of interest at the IF stage is defined as $S_{IF}(f)$ and the *Signal to Mixing Distortion Ratio* (SDmR) as follows:

$$SDmR = \frac{\int_{fIF-BW_{CH}/2}^{IF-BW_{CH}/2} |S_{IF}(f)|^2 df}{\int_{f_{IF}-BW_{CH}/2}^{f_{IF}-BW_{CH}/2} |D_I(f)+D_B(f)+D_{SRF}(f)|^2 df} \quad (6\text{-}1)$$

Where BW_{CH} is the occupied band by the useful information, i.e. the signal of interest. It is observed from (6-1) and from Figure 3-6 that if I(f) and B(f) can be filtered prior to sampling in order to attenuate the impact of $D_I(f)$ and $D_B(f)$, which relaxes L(Δf) specifications. On the other hand, $D_m(f)$ is proportional to the power of the signal of interest, where filtering cannot relax L(f) specifications.

Multiple mixing stages can actually relax phase noise specifications. Low f_{LO} (which usually presents better L(Δf) than high frequency f_{LO}) can be used for a first down-conversion. With a fixed IF, selective IF is used to reduce I(f) and B(f) powers for application of a second f_{LO} which is higher and contains poor L(Δf).

2.2 The Phase Noise Consideration in the Nyquist Sampling Operation

On the sampling process, the phase noise impact also depends on the oscillator phase noise, but also on the signal to be sampled center frequency. In this chapter we use f_0 for the signal of interest center frequency and f_I for an interferer center frequency. Into Nyquist or BPS sampling operation, classical clock and aperture jitter analysis is performed in [130-132]. For simplification, only the signal of interest is considered to be sampled. Let's consider a CT domain signal $s_c(t)$ being sampled in presence of jitter at instants $t=nT_s+\Delta_n$:

$$s_S(t) = \sum_{n=-\infty}^{\infty} s_C(t) \cdot \delta(t - nTs - \Delta_n) \quad (6\text{-}2)$$

After digitization of the signal, the actual sampling instant is unknown and considered uniformly distributed at nT_S. This operation is, by definition, the source of the jitter error:

$$s[n] = s_S(nTs + \Delta_n) = s_C(t) \cdot \delta(t - nTs - \Delta_n) \quad (6\text{-}3)$$

For simplicity and without lack of generality, the jitter influence is studied taking into account a sine wave defined as follows:

$$s(t) = A\cos(2\pi f_0 t) \tag{6-4}$$

The difference between $s_S(nTs)$ and $s_S(nTs+\Delta_n)$, which is the sampling jitter error ERRj is illustrated in Figure 6-2.

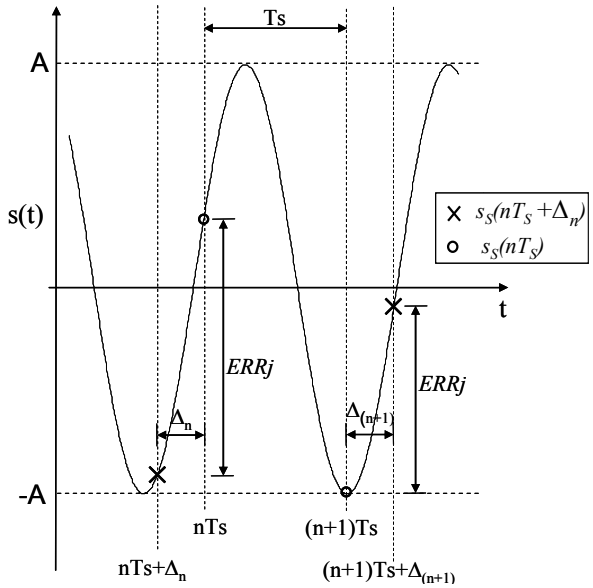


Figure 6-2 : The sampling operation in the presence of jitter

The error amplitude depends on the derivate of s(t) around nTs and the sampling instant deviation Δ_n :

$$s_S(nTs+\Delta_n) = s_S(nTs) + s_S'(nTs)\Delta_n = A\cos(2\pi f_0 nTs) - A2\pi f_0 \sin(2\pi f_0 (nT_S))\Delta_n \tag{6-5}$$

When Δ_n is an uncorrelated random process with a normal distribution and variance of σ^2, the derived SDjR is given by:

$$SDjR = \left[\frac{\cos(2\pi f_0 nT_S)}{2\pi f_0 \sin(2\pi f_0 nT_S)\cdot\sigma}\right]^2 \approx \left[\frac{1}{2\pi f_0 \sigma}\right]^2 \tag{6-6}$$

As expected, equation (6-6) confirms what has previously been stated, that the impact of phase noise on the sampling SDjR depends on the LO phase noise (translated into jitter variance σ^2) [133] and the signal center frequency f_0.

Yet, classical jitter analysis considers the SDjR evaluated into the total Nyquist band [0; fs/2]. Like the quantization error in over-sampled ADCs, the total jitter error PSD decreases when higher sampling frequencies are applied. Whenever ($fs >> 2\cdot BW_{CH}$) the jitter error PSD integrated within the band of interest, gives an error smaller than the total jitter error. A second limitation is that the jitter is often a correlated process, coming for example from the $1/f^2$ phase noise. On the following section we observe that in this case, the jitter distortion is concentrated around the sampled signal.

The presence of interferers and modulated signals at the input are two other aspects to take into account. In order to cover these points, a more precise method is then necessary which is developed on the next section.

2.3 The Bandpass Sampling System and Motivations for the Study

In the sampling process, the jitter comes from two different sources: one from oscillator $1/f^2$ phase noise and the other from aperture jitter (white phase noise) (Figure 6-3). The jitter from the LO is correlated, as presented in section 4.1 as the jitter variance cumulates over the time. In the frequency domain, it gives the phase noise PSD concentrated around f_{LO} ($1/f^2$ phase noise). In Figure 6-3, g(t) represents the sampling signal, which is a sequence of Dirac pulses with periodicity Ts but with deviations Δ_n:

$$g(t) = \sum_{n=-\infty}^{\infty} \delta(t - nTs - \Delta_n) \tag{6-7}$$

The BPS operates two distinct processes, the frequency conversion and the sampling; this actually merges the impact of phase noise in the mixing and in the Nyquist sampling operations. The SDjR must then be evaluated around the down-converted signal $f_{IF} = f_0 - Nfs$ (Figure 6-3), where N is the harmonic responsible for the down-conversion:

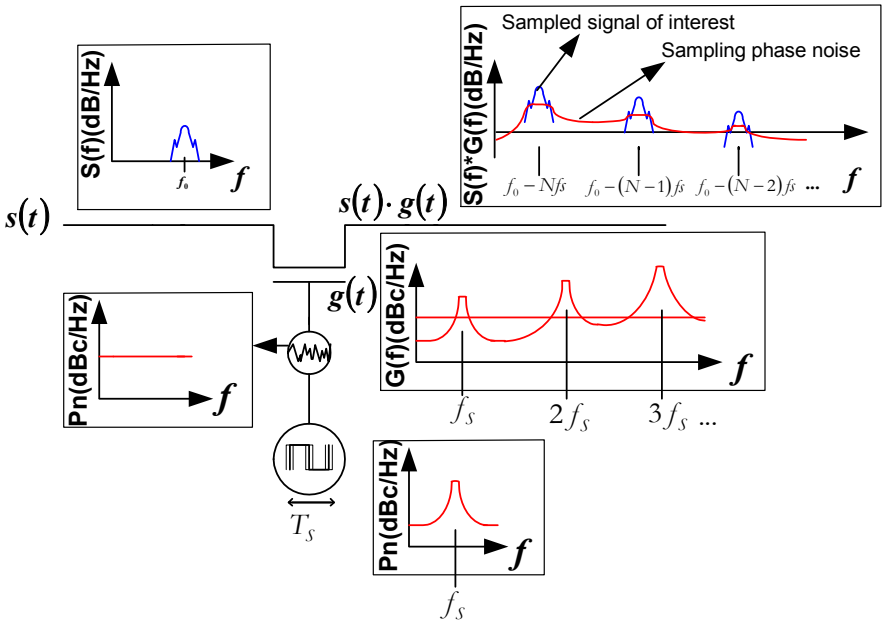


Figure 6-3 : Block diagram of a jittered sampling system and the different phase noise sources

The lack of information in the literature has motivated the development of a numerical method to specify phase noise in BPS systems, following these main steps:

- Modeling of precise phase noise distributions and therefore realistic jitter models.
- Evaluating the bandpass sampled SDjR within only the band of interest.
- Applying as inputs, modulated signals: The signal of interest and interferers.

On the following, a more in-depth study is carried out through analytical and numerical approaches. The results on the impact of phase noise into BPS are used to validate phase noise specifications and compare the differences between the BPS approach with classical mixing or sampling. The derived specifications can also give an idea if applying BPS can actually improve or worsen the power consumption performance for the frequency synthesis blocks.

3 The Jitter Impact Analysis

In this section we develop an analytical study concerning the BPS process in presence of jitter. The objective is to have a theoretical expression for the down-converted local SDjR for a first simple case test bench, where the jitter distribution is independent and stationary. This theoretical analysis presents an enhancement compared to Nyquist sampling jitter analysis and will serve as basis to calibrate and validate the numerical method. In this first study, the jitter distribution is considered non-correlated and gives relations for the phase noise floor specifications on the BPS process.

3.1 Analytical Approach - The Bandpass Sampling with Uncorrelated Jitter

In this section we derive the PSD for the jitter distortion in the BPS process. The SDjR is derived for a band of interest which is different than the Nyquist frequency, $BW_{CH} \neq fs/2$. The SDjR is evaluated in terms of the sampling frequency fs, the signal center frequency f_0 (relating to the under-sampling ratio N), the jitter limits $[-\beta;\beta]$ for the uniform distribution and the jitter variance σ^2 for the Gaussian distribution.

This analytical development is based on the non-uniform sampling theory [134]. First, we derive the PSD of a sequence composed by non-uniformly spaced Dirac pulses, indicated as G(f). More precisely, g(t) is a periodic Dirac pulses sequence of mean period set to Ts but with deviations from ideal sampling instants given by Δn (6-2). Then, S(f) is defined as PSD for the signal of interest.

The sampled signal PSD $S_S(f)$ is given by the convolution between S(f) and G(f):

$$S_S(f) = G(f) * S(f) \tag{6-8}$$

From Ss(f), we can distinguish the correlated part for the sampled signal of interest $S_{CORS}(f)$ and the sampling jitter distortion Dj(f) (Figure 6-3) when G(f) is known. We consider that the sampled signal occupies a band between f1 and f2. The resulting SDjR is given by the integrated PSD for the sampled signal of interest divided by the jitter distortion in the same band:

$$SDjR(f_1, f_2) = \frac{\int_{f1}^{f2} S_{CORS}(f)df}{\int_{f1}^{f2} Dj(f)df} \tag{6-9}$$

Based on the theoretical development given in [135], G(f) is (see detail in APPENDIX G):

$$G(f) = \frac{W(f)}{T_s^2} \sum_{n=-\infty}^{\infty} \delta\left(f - \frac{n}{T_s}\right) + \frac{1 - W(f)}{T_s} \tag{6-10}$$

The PSD of a non-uniformly distributed Dirac Pulses sequence is also known on the *Ultra Wide Band* (UWB) radio domain. Often, the spectrum is classified between the discrete

spectrum, called the spectral lines, and a continuous spectrum contribution. In (6-10), a periodic sequence of lines with period equal to 1/Ts is identified and attenuated by a weight function W(f), which is dependent on the distribution of Δn, defined above. The second term of (6-10) is the continuous spectrum part of G(f). Figure 6-28 illustrates S(f) and G(f), and the sampled and down-converted $S_S(f)$ (by the N^{th} harmonic) in a BPS process:

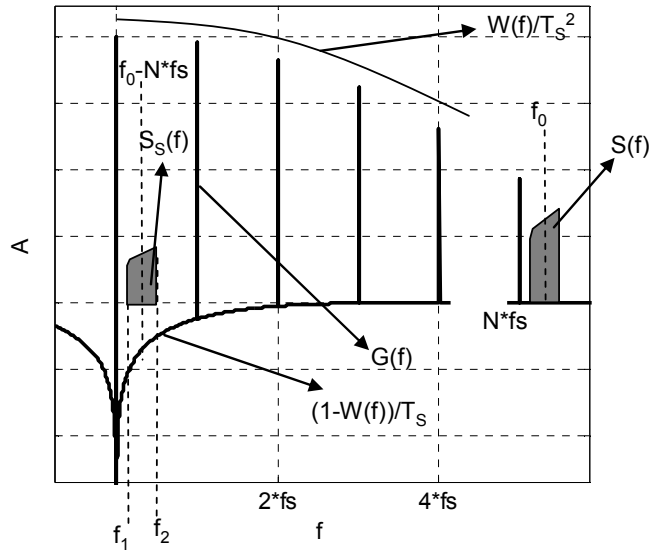


Figure 6-4 : Spectral representation of S(f), the sampled spectrum Ss(f) and G(f) for jittered BPS

The BPS process implements down-conversion and CT- to DT- domain conversion. The IF domain is the convolution between the N^{th} spectral line and signal of interest. Therefore, the PSD of the sampled signal of interest $S_{CORS}(f)$ is:

$$S_{CORS}(f) = \frac{W(N/Ts)}{T_S{}^2} \cdot S\left(f - \frac{N}{T_S}\right) \tag{6-11}$$

The weight function at N/Ts, W(N/Ts), represents an attenuation of the correlated part for the ideally sampled signal. The PSD of the sampled jitter distortion, Dj(f), is equal to the convolution product between the continuous spectrum of G(f), and S(f):

$$Dj(f) = S(f) * \left[\frac{1-W(f)}{T_S}\right] \tag{6-12}$$

The SDjR between f1 and f2 is derived applying (6-11) and (6-12) on (6-9):

$$SDjR(f_1, f_2) = \frac{\int_{f1}^{f2}\left\{\frac{W(N/Ts)}{T_S{}^2} \cdot S\left(f - \frac{N}{T_S}\right)\right\} df}{\int_{f1}^{f2}\left\{S(f) * \left[\frac{1-W(f)}{T_S}\right]\right\} df} \tag{6-13}$$

From Figure 6-14, the down-converted signal is defined f1 and f2 in the BPS process:

$$f_1 = f_0 - N/Ts - BW_{CH}/2$$
$$f_2 = f_0 - N/Ts + BW_{CH}/2 \tag{6-14}$$

The derivation of the BPS SDjR for this test bench is detailed in APPENDIX H , and a simplification considers that $BW_{CH} << f_0$, which leads to this simplified relation:

$$SDjR = \frac{1}{BW_{ch}} \frac{1}{78.9\sigma^2 f_0} \frac{1}{N} \tag{6-15}$$

Where σ^2 is the variance of the random process, which for uniform distribution with interval [-β;β], it means:

$$\sigma^2 = \frac{(2\beta)^2}{12} \tag{6-16}$$

Observe that for $N \approx f_0/fs$ the equation becomes:

$$SDjR = \frac{1}{78.9\sigma^2 f_0^2} \frac{fs}{BW_{CH}} \tag{6-17}$$

This equation shows that although the signal is under-sampled regarding f_0, the signal information (BW_{CH}) can be actually over-sampled $fs/(BW_{CH})$, therefore increase the SDjR. The jitter noise is flat from 0 to fs/2. Now consider equation (6-6) and the fact the jitter distortion PSD is integrated in the entire fs/2 band. The Gaussian aperture jitter presents a flat PSD from 0 to fs/2. The jitter PSD is given by:

$$Dj(f) = (2\pi f_0 \sigma)^2 \frac{fs}{2} \tag{6-18}$$

And the jitter distortion for a given BW_{CH} is given by:

$$Dj(f) = (2\pi f_0 \sigma)^2 \frac{2}{fs \cdot BW_{CH}} \tag{6-19}$$

Therefore the SDjR for a given bandwidth calculated from (6-6) gives the same result as (6-17):

$$SDjR = \frac{1}{2 \cdot (2\pi)^2 \sigma^2 f_0^2} \frac{fs}{BW_{CH}} = \frac{1}{78.9 \cdot \sigma^2 f_0^2} \tag{6-20}$$

The results obtained here can be compared to the quantization noise, where an over-sampling ratio can increase the resulting SNR. The difference is that the distortion power is also dependent on the signal to be sampled amplitude and derivate, i.e. the signal to be sampled center frequency.

The noise depends on the interferer amplitude A_I, as in the quantization noise, the difference between the signal of interest amplitude A_S and A_I is considered on the ADC SNR. Consider the BPS with jitter for an input which contains the signal of interest and an interferer, with amplitude A_I and center frequency f_I. If $A_I > A_S$ and $f_I > f_0$, the jitter distortion is mostly dependent on the interferer and not on the signal of interest. The detailed development is presented in APPENDIX H , and the resulting BPS SDjR is obtained in the presence of an interferer is given by:

$$SDjR = \frac{A_S^2}{A_I^2} \frac{1}{78.9 \cdot \sigma^2 \cdot f_I^2} \frac{fs}{BW_{CH}} \tag{6-21}$$

These results show the dependence of the SDjR to the sub-sampling ratio 2·N and not only to the signal center frequency and BW. Later, we see that it is not the case for the correlated jitter, as the following numerical method will illustrate.

3.2 Numerical Approach to Analyze Arbitrary Phase Noise Impact on Bandpass Sampling

The development of this numerical approach is motivated by the evaluation of different jitter distributions (from PLL/DLL models) impact on modulated BPS signals. We analyze the SDjR in frequency domain, but the method is also adapted to data flow simulation. *Error Vector Magnitude* (EVM) and *Bit Error Rate* (BER) results can be derived through this method.

We remind equation (6-2) which defines the sampled signal in the presence of jitter:

$$s_S(t) = \sum_{n=-\infty}^{\infty} s_C(t) \cdot \delta(t - nTs - \Delta_n) \tag{6-22}$$

Therefore, after digitization, the signal is considered as it was uniformly sampled (this is by definition the source of the jitter error):

$$s[n] = s_S(nTs + \Delta_n) = s_C(t) \cdot \delta(t - nTs - \Delta_n) \tag{6-23}$$

The instantaneous jitter error is given by:

$$ERRj = s_S(nTs) - s_S(nTs + \Delta_n) \tag{6-24}$$

We define a second signal in CT domain $\overline{s_C}(t)$ which is uniformly sampled at instants $t=nT_S$:

$$\overline{s_S}(t) = \sum_{n=-\infty}^{\infty} \overline{s_C}(t) \cdot \delta(t - nTs) \tag{6-25}$$

$$\overline{s}[n] = \overline{s_S}(nTs) = \overline{s_C}(t) \cdot \delta(t - nTs) \tag{6-26}$$

$\overline{s_S}[n]$ is defined such as $\overline{s_S}[n] = s[n]$. This means that $\overline{s_S}(t)$ is a distorted version of $s_S(t)$:

$$\overline{s_s}(nTs) = s_s(nTs + \Delta_n) \tag{6-27}$$

The different signals are then defined in Figure 6-5:

- $s_C(t)$ = CT signal to be sampled in the simulation
- $s_S(mT_{res})$ = the DT representation of $s_C(t)$ in a simulation environment where the time step is defined to be T_{res}
- $s_S(nT_S + \Delta n)$ = sampled signal of $s_C(t)$ in presence of jitter Δn
- $\overline{s_S}(nT_S)$ = the uniformly sampled signal with sampling period Ts of the distorted signal defined in (6-27)

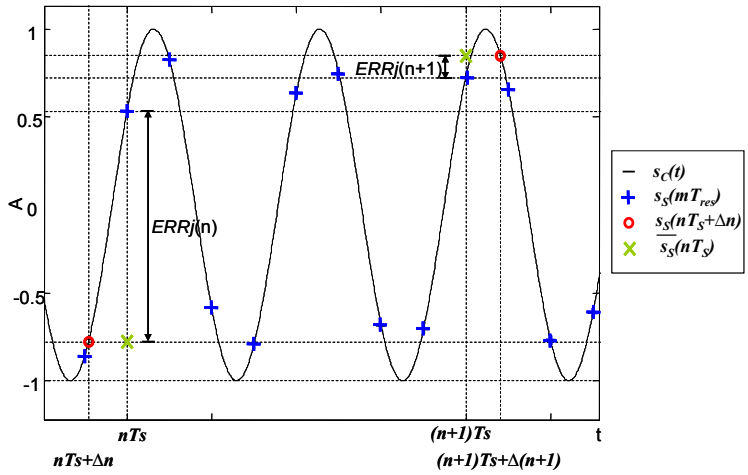


Figure 6-5 : The interpolation representation and the sampling instants

As illustrated in Figure 6-5, in order to find $\overline{s_S}(nT_S)$, the function $s_C(t)$ must be defined for every $t=(nTs+\Delta_n)$, i.e. analytical signal. We observe that, from Figure 6-5, the signal $s_S(mT_{res})$ is not defined for every $t=(nTs+\Delta_n)$. When $s_C(t)$ is analytical, $s_C(t)$ can be calculated for every $t=(nTs+\Delta_n)$, and Δ_n can be any value, which means that any jitter variance can be evaluated.

Consider a simulation environment where $s_C(t)$ is not an analytical function (ex: random data transmission) evaluated in DT domain at the instants $t=mT_{res}$, where T_{res} is the time resolution for the simulator. The signal $s_C(t)$ is unknown for $t \neq mT_{res}$. In such cases, the time instants $t=nTs+\Delta_n$ be defined within mT_{res}. Therefore, to accurately simulate the impact of Δ_n corresponding to a random process with variance σ^2 then $T_{res} << \sigma^2$. In most cases, this analysis becomes impractical for some simulated time intervals (ex: BER calculations).

Therefore we use a technique to calculate the accurate value of $s_C(t)$ for $t=nTs+\Delta_n$ through sinus cardinal interpolation [7]. We remind the classical interpolation equation:

$$s_C(t) = \sum_{K=-\infty}^{\infty} s_S[K] \frac{\sin[\pi(t-KTs)/T_S]}{[\pi(t-KTs)/T_S]} \tag{6-28}$$

The signal $S_C(f)$ must be band limited from $-f_{res}/2$ to $f_{res}/2$.

The numerical method steps are the following:

- We consider the signal $S_S(nTs)$, nTs is defined inside mT_{res}.
- Around nTs, a finite sequence (2·L points) of the signal around $s_S(nTs)$ is considering for the interpolation.
- The interpolation is applied to calculate the value of $s_C(t)$ for $t=nTs+\Delta_n$.

The reconstructed value is:

$$\overline{s_S}(nT_S) = s_C(nT_S + \Delta_n) = \sum_{K=-L}^{L} s_S[Ts(K+n)] \frac{\sin[\pi(\Delta_n - KTs)/T_S]}{[\pi(\Delta_n - KTs)/T_S]} \tag{6-29}$$

Since the sequence is finite containing 2L points, an interpolation error is introduced. The choice of the number of samples for interpolation 2L, is a trade-off between calculation time and interpolation error.

In order to define the allowed interpolation error, it is important to set the application environment of the method. In our case, the standards application environment is the ULP RF standards, BT-LE and IEEE802.15.4. The required SNDR for a given BER and modulation type are defined in Chapter 3, and the most constraining specifications are for BT-LE which SNDR=14dB. In this context, the required SDjR to be evaluated is around SDjR=40dB. An interpolation error of ERRint < -50dBc leads to a SDjR resolution of ±0.5dB for SDjR=40dB.

In order to evaluate the SDjR within a band of interest, first the error defined in (6-24) is calculated. To calculate ERRj, an hypothesis is set: the system is time invariant. This assumption allows us to affirm that the sampled signal contains two spectral components, where one is correlated with the ideally sampled signal and the second is the jitter distortion, non-correlated with the signal. To separate these two components and evaluate the total SDjR into a given frequency band, the Bussgang Theorem [108, 136] is applied.

Let's define $\overline{S_S}(f)$ as the DSP of the sampled signal in presence of jitter calculated from the numerical method and $S_S(f)$ the DSP from the ideally sampled signal. The correlation factor A between these two signals, inside the band of interest [f1;f2], is given by:

$$A = \int_{f1}^{f2} \frac{\overline{S_S}(f) \cdot S_S^*(f)}{S_S(f) \cdot S_S^*(f)} df = \frac{\left\langle \overline{S_S}, S_S^* \right\rangle}{\|S_S\|^2} \tag{6-30}$$

The correlated part defining the sampled signal of interest $S_{CORS}(f)$ has been defined in 3.1 and on the numerical method, it represents the part of the BPS sampled signal which is correlated with the ideally sampled signal $S_S(f)$. The definition of the jitter distortion Dj(f) is also present 3.1. On the method it represents the uncorrelated part between the BPS signal $\overline{S_S}(f)$ and $S_S(f)$:

$$S_{CORS}(f) = A^* \cdot S_S(f) \tag{6-31}$$

$$Dj(f) = \overline{S_S}(f) - S_S(f) \tag{6-32}$$

The total SDjR within [f1;f2] is then calculated:

$$SDjR = \int_{f1}^{f2} \frac{S_{CORS}(f) \cdot S_{CORS}^*(f)}{Dj(f) \cdot Dj^*(f)} df = \frac{\|S_{CORS}\|^2}{\|Dj\|^2} \tag{6-33}$$

In order to compare with the theoretical results, calibrate and validate the method, a simple test bench is used. A cosine input signal is chosen, and in this way $s_C(t)$ can be analytically defined for every $t=nTs+\Delta_n$. The cosine input also allows comparison between our numerical method and the analytically derived SDjR on section 3.1.

The simulated results are compared the analytical results from 3.1 (6-15) and the SDjR calculated through (6-33). In a first step, $\overline{s_S}(nT_S)$ is analytically calculated. The error between the analytically defined $\overline{s_S}(nT_S)$ and the one obtained through interpolation defines the interpolation resolution for a given number of samples 2L. Table 6-1 summarizes the applied test bench. The signal is centered at f_0 = 510MHz and the sampling frequencies vary from fs=100MHz to fs=500MHz. Different sampling frequencies are applied while the distance f_0-Nfs =10MHz is kept constant to evaluate the SDjR in the same [f1;f2] interval. Table 6-2 summarizes the evaluated SDjR.

$T_{res} = 250\,ps$
$f_1 = 9.3MHz$
$f_2 = 10.7MHz$
$s_C(t) = 1 \cdot \cos(2\pi 510x10^6 t)$
$\sqrt{\sigma^2}_A = 10\,ps$
$\sqrt{\sigma^2}_B = 20\,ps$

Table 6-1 : Test bench application summary

The SDjR is evaluated on a range from 39dB to 53dB with interpolation errors below -53.8dBc, which validates the method for the proposed application. The resulting number of points for the interpolation is L=10. In conclusion, this technique is able to calculate $S_S(nTs+\Delta n)$ for $\Delta_n < T_{res}$ for arbitrary $s_c(t)$ in the condition that S(f) is a band limited signal. It is also noticeable that no limitation is presented through the application of Δ_n which can be calculated from correlated and non-correlated jitter distributions. Some case studies are applied in

order to perform a more in-depth analysis on the impact of phase noise on BPS process. Aspects of such correlated phase noise, wideband phase noise and modulated signal are introduced on the following section.

	(6-15)		$\bar{s}_S(nTs)$ analytic		$\bar{s}_S(nTs)$ interpolated		PSD Estimation error (-dBc)		Interpolation Error (-dBc)	
σ	10ps	20ps	10ps	20ps	10ps	20ps	10ps	20ps	10ps	20ps
SDjR(dB) @ fs=100MHz	45.41	39.4	45.54	39.56	45.69	39.69	-60.7	-53.8	-60.2	-54.5
SDjR(dB) @ fs=125MHz	46.38	40.37	46.55	40.99	46.68	41.13	-60.5	-49.1	-61.8	-55.9
SDjR(dB) @ fs=250MHz	49.39	43.38	49.4	43.54	49.52	43.67	-75.8	-57.8	-65.1	-58.9
SDjR(dB) @ fs=500MHz	52.4	46.39	52.89	46.6	53.03	46.74	-62.1	-59.6	-67.9	-61.6

Table 6-2 : SDjR x *fs* for the different techniques

4 Case Studies

In the previous sections, we presented the context of the phase noise impact in a receiver and in particular the impact of phase noise on the BPS process. The analytical approach presents a simplistic test bench. This method is compared and validated the analytical approach.

On the following, different test benches, regarding different modulations, different signal center frequencies f_0 and sampling frequencies fs with a more realistic jitter model will be studied. The first step of this study is to propose jitter models for the PLL and DLL based on what is presented in [137]. Since this method is to validate the phase noise for ULP RF standards, GFSK (BT-LE) modulation is used in our case studies.

Since the presence of spurious in PLL and DLL is a serious problem limiting the block design performances, this phenomenon is added on the top of jitter model and its impact on BPS SDjR is studied. The results coming from this section will be used as charts and trends. The last section is dedicated to perform the system level specification and validation for the phase noise in BPS process for the proposed architecture described in Chapter 4 and the ULP RF standards.

4.1 Method Applied on a GFSK Modulated Signal in Presence of Aperture Jitter Combined with Synthesis Jitter

Initially we derive the jitter model to be applied in the method. After, we present a test bench which illustrates the differences between the correlated jitter impact and the non-correlated jitter one. The jittered sampling instants are calculated for a locked LO which phase noise is L(f) is [129] :

$$L(f)=\left[\frac{f_{lo}{}^{2}c}{(f-f_{lo})^{2}+\pi^{2}f_{lo}{}^{4}c^{2}}\right]\cdot H(f) \tag{6-34}$$

The function H(f) is the PLL loop frequency response. On the following, we describe how to obtain a jitter sequence which represents the spectrum of (6-34). In a running free oscillator, the jitter variance increases along the time (Figure 6-6):

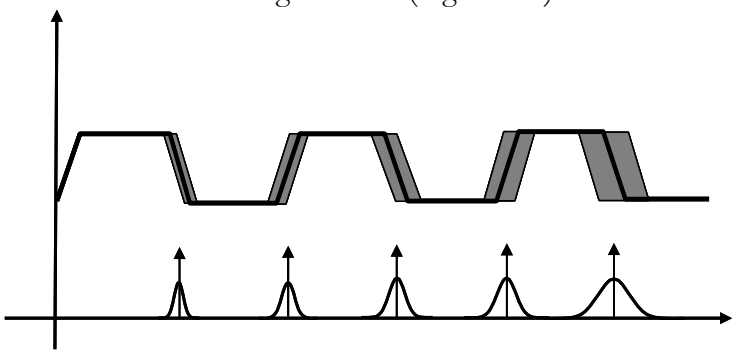


Figure 6-6 : The cumulative effect on LO jitter variance

Consider an ideal oscillator $V_{LO}(t)$. The zero-crossing points on the signal are defined at nT_{LO}, where T_{LO} is the LO period. In presence of jitter the zero-crossing points deviates to $nT_{LO}+\Delta_n$. It is observed in Figure 6-6 that the next zero-crossing point is dependent on the last one, which makes the process variance to increase over the time. The absolute jitter at an instant t is given as follows:

$$\sigma_{abs}{}^{2}(t)=c\cdot t \tag{6-35}$$

The variance accumulation over the time can be described as a *Wienner* process [138] where the next value on a random distribution depends on the last value. "c" can be interpreted as the rate the jitter variance increases over time and is directly related to the *Voltage Controlled Oscillator* (VCO) performance, independently from the used VCO frequency. Another useful parameter to be defined is the cyclic jitter, which is the cumulated jitter variance over one period T_{LO}:

$$\sigma_{c}{}^{2}=c\cdot T_{LO} \tag{6-36}$$

In a PLL or DLL the phase error is corrected in a phase- or delay- comparator with a reference oscillator, which jitter is much lower compared to the VCO one. This phase correction leads to the locked oscillator which is obtained by filtering with H(f) the previously described *Wienner* process. The limitation of the model is that is does not consider the phase noise coming from the reference, which is considered ideal.

As a result of the phase correction, the long term jitter becomes finite, defined as *Root Mean Square* (RMS) jitter or tracking jitter $\sigma_{rms}{}^{2}$:

$$\sigma_{abs}{}^{2}(t)\big|_{t\to\infty}=\sigma_{rms}{}^{2} \tag{6-37}$$

Figure 6-7 illustrates the linear model for the phase transfer function in a PLL / DLL type. We are interested in investigating the transfer function between the VCO phase noise ϕ_{nVCO} and the PLL / DLL phase output ϕ_{out} [139].

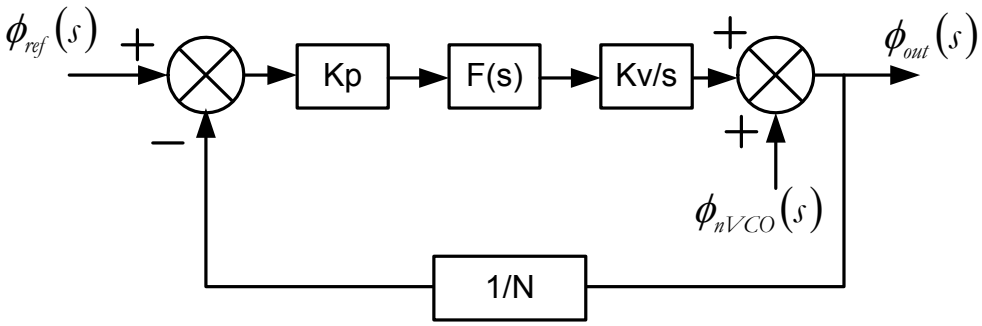


Figure 6-7 : The PPL / DLL linear model

Based on Figure 6-7, this relation is as follows:

$$\frac{\phi_{out}}{\phi_{nVCO}}(s) = \frac{N}{K \cdot F(s)} \cdot \frac{s}{\frac{s \cdot N}{K \cdot F(s)} - 1} \qquad K = Kp \cdot Kv \tag{6-38}$$

F(s) is the phase detector charge pump filter. Typically F(s) is a first order low-pass filter, the ϕ_{out}/ϕ_{nVCO} becomes a second order high-pass filter for the VCO phase noise:

$$Kp \cdot F(s) = \frac{RCs + 1}{Cs} \tag{6-39}$$

$$\frac{\phi_{out}}{\phi_{nVCO}}(s) = \frac{s^2}{s^2 + 2s\xi\omega_n + \omega_n^2} \qquad \omega_n = \sqrt{\frac{K}{2\pi C \cdot N}} \qquad \xi = \frac{R}{2} \cdot \sqrt{\frac{C \cdot K}{2\pi \cdot N}} \tag{6-40}$$

This leads to a phase noise type which decreases 20 dB/dec from $\Delta f = f_n = \omega_n/2\pi$ to $\Delta f = 0$ (Figure 6-8). Actually, other blocks inside the PLL/DLL (*Frequency Divider* (FD), latch combiner, *Phase-frequency Detector Charge Pump* (PDCP) and the reference) also generate noise which makes the phase noise from fn to f_0 approximately flat ([139] (Figure 6-9)). The noise generated by the FD and PDCP have a non-correlated white noise behavior. For the loop, the output phase noise PSD from the frequency divider is amplified by N and then low-pass filtered.

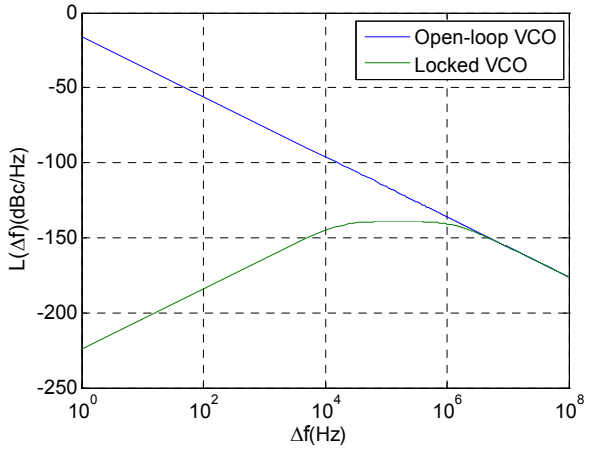


Figure 6-8 : The VCO phase noise

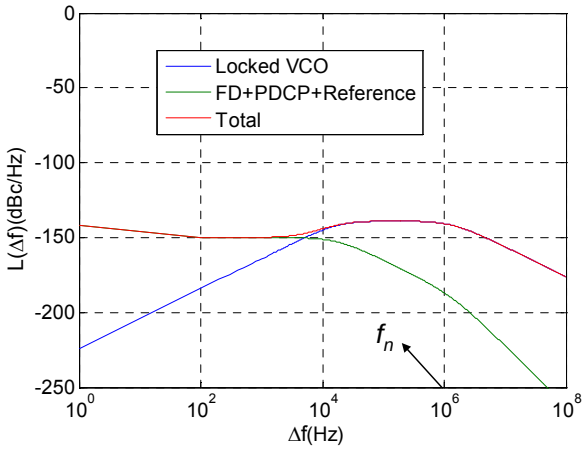


Figure 6-9 : The total PPL / DLL phase noise

In order to better approximate the RMS jitter of real PLL, we model the jitter as being a *Wiener* process filtered by a first order high-pass filter. The long term jitter or jitter RMS can be inferred from the total integrated phase noise PSD from Figure 6-9 ([140]), and for a first order loop PLL, the RMS jitter is given as follows:

$$\sigma_{rms}^2 = \left(\sigma_c^2 f_{lo}\right)\frac{1}{\omega_n} \tag{6-41}$$

The first order high-pass filter can also be used for DLL frequency synthesis type. The jitter variance is cumulated over N (multiplication ratio) periods and reset through phase comparison; this limits the jitter variance accumulation over the time. As in the PLL, the DLL locked loop bandwidth also depends on the reference frequency and on stability criteria [141]. We define the following steps to generate the timing jitter which represents the phase noise of (6-34). From the spectral density far from ω_n (Figure 6-9), the parameter "c" is derived for an open-loop oscillator. Then, the random noise described by the *Wienner* process is generated and filtered by a first order high-pass filter with cut-off frequency f_n. When it is needed to include the aperture jitter on the generated sequence, a Gaussian non-correlated jitter is added to the synthesis jitter. We define a test bench where the input is a GFSK modulated signal M(t), according to BT-LE standard. The bandwidth @ -30dBc is BW_{CH}=1.25MHz. Random data is generated and the proposed numerical method to calculate $\overline{s_S}(nTs)$ is applied.

Tres	f1	f2	sC(t)	fn	σrms
250ps	9.3MHz	10.7MHz	M(t).cos(2π.510x106t)	1MHz	45ps

Table 6-3 summarizes the test bench applied in this case:

T_{res}	f_1	f_2	$s_C(t)$	f_n	σ_{rms}
250ps	9.3MHz	10.7MHz	M(t)·cos(2π·510x10^6t)	1MHz	45ps

Table 6-3 : Test bench application summary

where $M(t) = I(t)\cos(2\pi f_0 t) - Q(t)\sin(2\pi f_0 t)$. The jitter type is a PLL based with fixed f_n and "c", therefore σ_{rms}^2 is kept constant. The process is evaluated applying the following sampling frequencies:

$$f_s = 50MHz,\ 100MHz,\ 250MHz\ \ 500MHz$$

Figure 5-29 shows the BPS signal of interest $S_{CORS}(f)$ and the jitter distortion Dj(f). We verify the jitter distortion is localized around the sampled signal center frequency. Figure 6-11 illustrates the jitter distortion for the different sampling frequencies defined in the given test benches. We observed the similar impact on the local SDjR for the different sampling frequencies. The SDjR is evaluated using (6-33) from f1 to f2 and the same SDjR=20.7dB is obtained for all test cases.

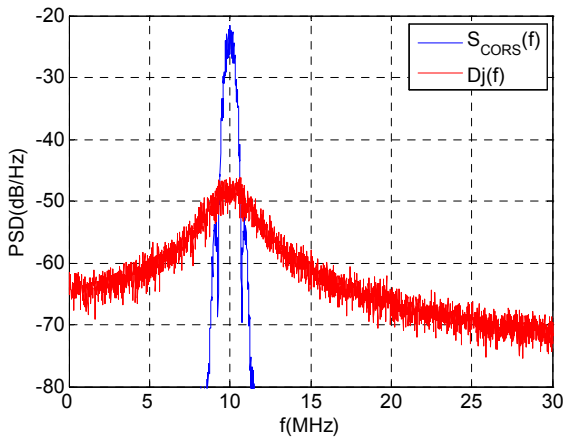


Figure 6-10 : $S_{CORS}(f)$ and Dj(f) @ fs=100MHz

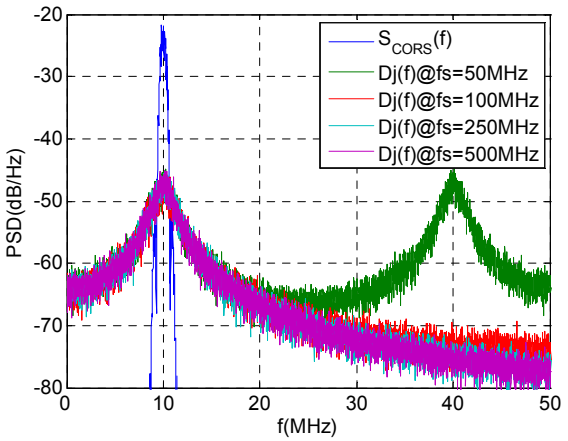


Figure 6-11 : $S_{CORS}(f)$ and Dj(f)

On the other hand, the in-band phase noise is strongly related to the PLL f_n to signal bandwidth ratio f_n/BW_{CH}. This can be observed in Figure 6-12 when the same f_0=510MHz and fs=100MHz and σ_{rms}=45ps are applied, for different fn. Although Dj(f) integrated from [0;fs/2] gives the same amount of distortion power, the Dj(f) becomes distributed outside the band of interest, which leads to better local SDjR when f_n increases.

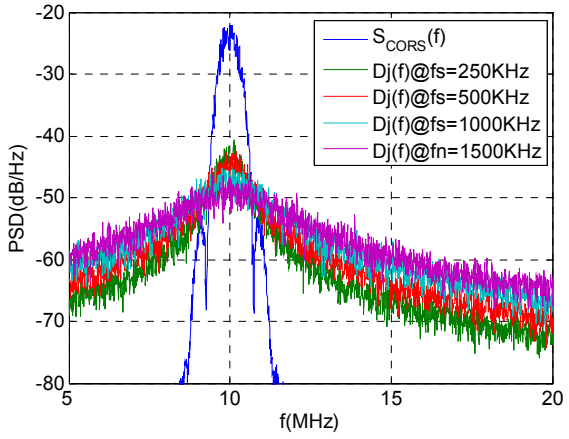


Figure 6-12 : $S_{CORS}(f)$ and Dj(f) @ fs=100MHz

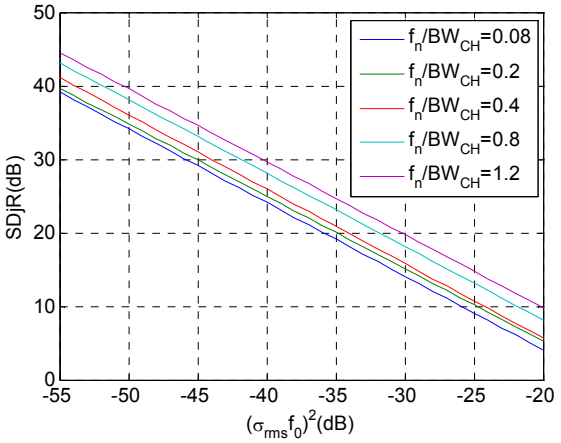


Figure 6-13 : SDjR x $(\sigma_{rms}\, f_0)^2$ for different f_n /BW_{ch}

In order to define an approximation on the SDjR considering a modulated signal and the proposed synthesis jitter model, the following test bench of Table 6-4 has been implemented. The results are detailed in Figure 6-13.

T_{res}	f_1	f_2	$s_C(t)$	fs	f_n/BW_{CH}
250ps	9.3MHz	10.7MHz	$M(t)\cdot\cos(2\pi\cdot 510x10^6 t)$	100MHz	[0.08 0.2 0.4 0.8 1.2]

Table 6-4 : Test bench application summary

We observe from Figure 6-12 that better SDjR is achieved for higher f_n with constant σ_{rms}^2. The PSD for the jitter distortion can increase outside the band of interesting with no harmful impact on the SDjR, thus relaxing phase noise specifications. Figure 6-13 shows the increase of the SDjR applying higher f_n.

The SDjR from the PLL jitter is proportional to $(\sigma_{rms}f_0)^2$ and f_n/BW_{CH} (Figure 6-13) and it does not vary with the sampling frequency as observed in Figure 6-11. We derive from Figure 6-13 an empirical expression which relates $(\sigma_{rms}f_0)^2$, f_n/BW_{CH} and SDjR:

$$10\log(SDjR) = -20\log(\sigma_{rms} f_0) + \theta\frac{f_n}{BW_{CH}} + \beta \qquad (6\text{-}42)$$

$$\theta = 5.09 \qquad \beta = -16.08$$

We observe the similarities between (6-20) and (6-42), where SDjR is linearly proportional to $1/(\sigma_{rms}f_0)^2$. In addition, the logarithm of SDjR is proportional to fn/BW_{CH}, and from Figure 6-13 we derive the coefficients θ and β.

The cut-off frequency f_n is limited at the block level by the stability criterion and the reference frequency f_{ref} (typically $f_n=f_{ref}/10$). Consider a non-fractional PLL where the frequency step is equal to the reference frequency $f_{step}=f_{ref}$. In order to address both BT-LE and IEEE802.15.4 channels, the frequency step of the PLL should be as low as f_{step}=1MHz; hence

f_n=100KHz. Considering the IEEE802.15.4 channel bandwidth, BW_{CH}=2.45MHz, it leads to f_n/BW_{CH} = 0.05. The low f_n/BW_{CH} ratio is a strong for multi-standard frequency synthesis blocks.

For the aperture jitter, we define σ_{AP}^2 as the variance of the random process which generates white phase noise. As observed in (6-20), the SDjR depends on the sampling frequency, which is not the case for the synthesis jitter SDjR. In Figure 6-14, we observe the SDjR x fs for the both synthesis and aperture jitter.

We observe in Figure 6-14 the impact of both the synthesis and aperture jitter. The contributions on the SDjR from the different jitter sources are the same on the crossing point indicated in Figure 6-14. Below this sampling frequency, the jitter distortion from the aperture jitter becomes higher than the synthesis jitter and we observe a dependency of the SDjR to the frequency. Above this frequency, the synthesis jitter impact is predominant and no dependency to fs is observed.

Next section we analyze the impact BPS SDjR in a test bench in presence of interferer. The 1/f phase noise and the presence of spurs are considered on the jitter model.

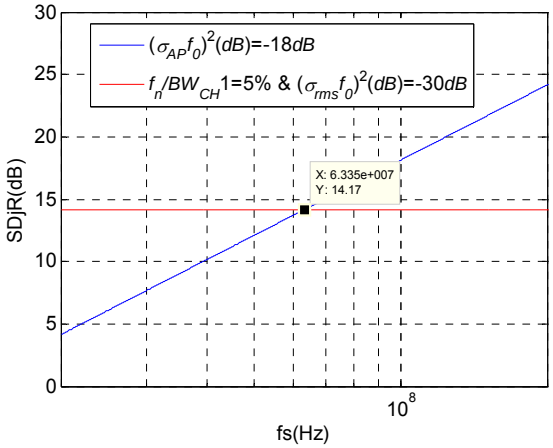


Figure 6-14 : SNDR x fs for different σ_{APP} and σ_c contributions

4.2 Jitter Analysis in Presence of Interferer

In section 2.1, the impact on the SDjR in presence of interferer is the most constraining case to define phase noise specifications. The jitter distortion for correlated sources is concentrated around the bandpass sampled signal, and follows a $1/f^2$ for frequency distances $\Delta f > fn$ (Figure 5-29). In this section, we introduce an interferer distanced Δf from the signal of interest $\Delta f = f_I - f_0$, and its impact on the sampling SDjR. The ratio between the interferer power P_I and the signal of interest power P_S is defined as $\Delta_P = P_I/Ps$.

4.2.1 Reciprocal Mixing Analogy

On the BPS process, the impact of the phase noise in the presence of an interferer is similar to the reciprocal mixing presented in 2.1. Differently from the mixing process, the

interference center frequency f_I must also be considered, since the jitter distortion is dependent on the signal center frequency (see section 3.1).

A first order high-pass filtered synthesis jitter is applied to analyze the impact of phase noise on BPS in the presence of interferer. Table 6-5 summarizes the applied test bench:

f_1	f_2	$s_C(t)$	fs	f_n	σ_{rms}
9.3MHz	10.7MHz	$M(t)\cdot\cos(2\pi\cdot510x10^6t)$	100MHz	1MHz	50ps

Table 6-5 : Test bench application summary

Figure 6-15 illustrates the PSD for the jitter distortion and the signal of interest after sampling; the derived SDjR is SDj_1R=20.3dB. We apply the same jitter considering the signal of interest and an interferer at the input. Figure 6-16 illustrates the PSD of the jitter distortion and the sampled signals. The frequency distance is Δf=4MHz and Δ_P =14dB. In this case, the derived SDjR is SDj_2R=15.72dB.

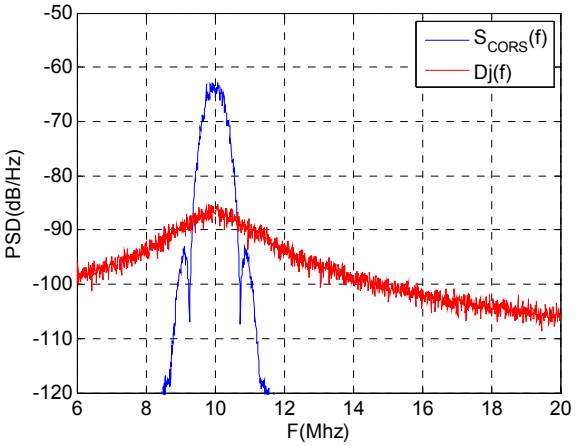


Figure 6-15 : Spectra of the sampled signal and jitter distortion

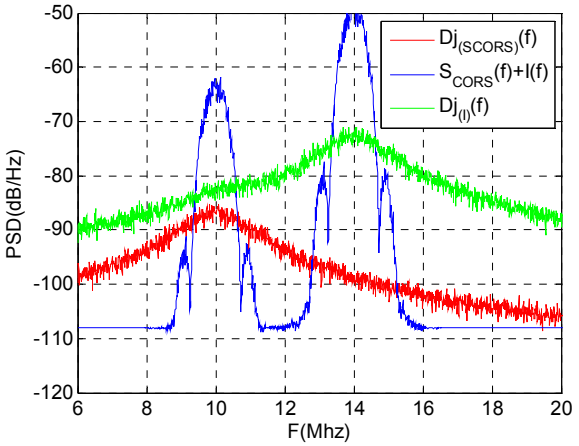


Figure 6-16 : Spectra of the sampled signal and jitter distortion

We observe from Figure 6-16 that the jitter distortion of the interferer $Dj_{(I)}(f)$ spreads along the frequency and degrades the SDjR. This distortion is often being stronger than the jitter distortion of the signal of interest ($Dj_{(SCORS)}(f)$ on Figure 6-16).

The interferers profile is defined in standards specifications and is summarized in Chapter 3. In a receiver, the ratio Δ_P will depend on the specifications and on the interferer rejection implemented before sampling.

The numerical method is applied to analyze the SDjR for different Δ_P (Δ_P=0 to 30dB) and Δf (Δf=1MHz to 5MHz). Table 6-5 defines the jitter parameters. Figure 6-17 illustrates the resulting SDjR. From these results,, we derive a semi-empirical expression to define the SDjR in the presence of interferer. For strong Δ_p the SDjR depends only on the interferer and in this case, the $DjR_{(SCORS)}(f)$ is negligible. In addition to the jitter variance and the signal center frequency, the SDjR is proportional to $1/(\Delta f)^2$ and Δ_p.

Similarly to the reciprocal mixing, the phase noise at Δf L(Δf) defines the $Dj_I(f)$. Since in the sampling process the distortion is proportional to the signal to be sampled derivate (6-5), the

distortion is proportional to the interferer center frequency. The specifications in phase noise are therefore referred to the interferer center frequency (see details in APPENDIX J):

$$L_{fs}(\Delta f)=\left(\frac{fs}{f_I}\right)^2 L_{fl}(\Delta f) \tag{6-43}$$

$$SDjR\cdot\Delta_p \div \left(\frac{1}{L(\Delta f)\cdot\frac{f_I^{\,2}}{fs^2}}\right) \Leftrightarrow SDjR\cdot\Delta_p \div \left(\frac{1}{L_{fl}(\Delta f)}\right) \tag{6-44}$$

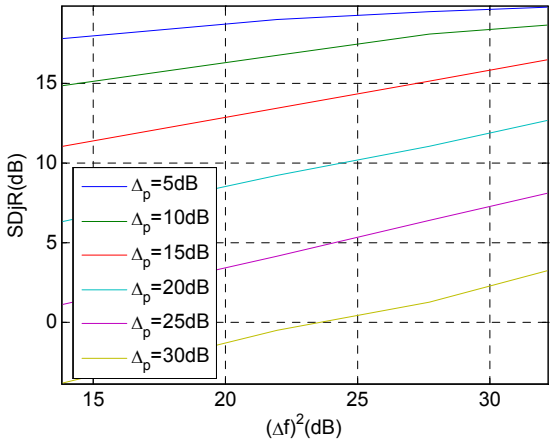


Figure 6-17 : SDjR x Δf^2

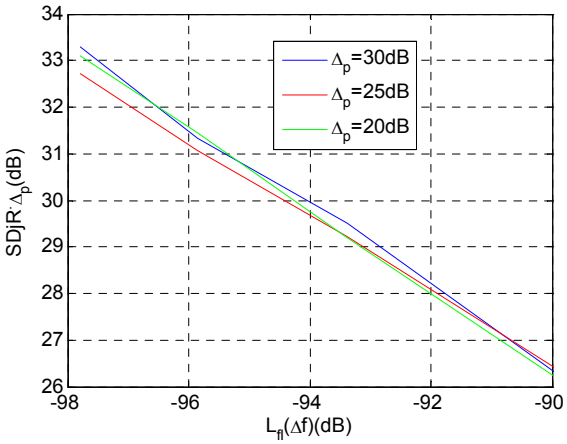


Figure 6-18 : SDjR·Δ_p x $L_{FI(\Delta f)}$

Figure 6-18 illustrates the relation between the SDjRxΔ_p product a $L_{fl}(\Delta f)$, which means that the phase noise is referred to the interferer center frequency. $L_{fl}(\Delta f)$ is calculated using the jitter parameters of Table 6-5 and expressions (6-34), (6-36) and (6-41).

The following relation is derived:

$$10\log(SDjR)=10\log\left(\frac{1}{L_{fl}(\Delta f)}\cdot\frac{1}{\Delta_p}\right)\cdot\theta+\beta \tag{6-45}$$

$$\theta=0.88 \qquad \beta=-50.28$$

The result of (6-45) is a first approximation reference for the phase noise specification in the presence of jitter. While using the proposed numerical method, successive simulations define the required phase noise for an SDjR specification. In this section we verify the impact of the interferers on the jittered BPS process. From Figure 6-16 we observe that the SDjR can be completely dependent on the interferer center frequency and power, despite the signal of interest. In the next section we add the spurious on the frequency synthesis modeling to analyze its impact on the BPS on the SDjR in presence of interferer.

4.2.2 Effect of Phase Noise Spurious on the BPS and the Presence of Interferers

The presence of harmonic spurious on multiples of the reference frequency is well-known on the PLL/DLL phase noise. In DLL frequency synthesis type, these spurs are caused by a static delay error between the last delay cell and the reference (Figure 6-19). This error can be caused by a mismatch between the paths which control the phase comparator, and

mismatches in charge pump. The most constraining spurs are the closest to the LO, and their level is proportional to the static error over the reference period ratio $\Delta T/T_{ref}$. In [142], the spurious power for different $\Delta T/T_{ref}$ and the number of delay cells is found. When the spur pops up way over the phase noise, it becomes the most constraining source of jitter distortion in presence of interferers. A modulated phase is added on the phase noise vector in order model the spurs:

$$\phi(t) = m\sin(2\pi f_{ref}) \tag{6-46}$$

The modulation index m defines the spurious level, and it is calculated through Bessel function of first kind $J_\alpha(m)$ for first and second order (α=1 and 2). The ratio between the carrier and the first spur Δ_{spur} is given by:

$$\Delta_{spur}(m) = 20\log 10\left(\frac{J_1(m)}{J_2(m)}\right) \tag{6-47}$$

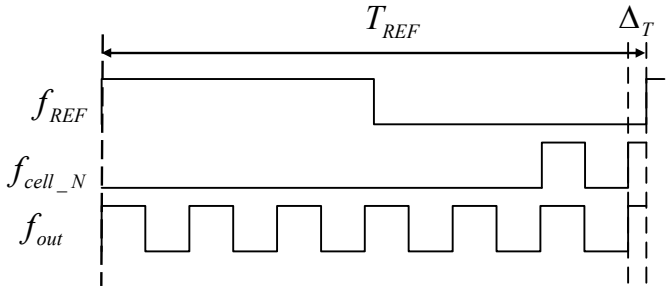


Figure 6-19 : The static delay error Δ_T in DLL

The phase variation is added on top of the random phase noise from the first order PLL/DLL. First a given $\Delta T/T_{ref}$ is set, which leads to a resulting spur level. From (6-47), m is calculated, which is applied on (6-46) to reproduce the spurs on the phase noise. The jitter generated on the previous test bench is reused in this study case in addition to the spur (results on Figure 6-20)

f_1	f_2	$s_C(t)$	fs	f_n	σ_{rms}	Δ_{spur}	f_{ref}
9.3MHz	10.7MHz	$M(t)\cdot\cos(2\pi\cdot510x10^6t)$	100MHz	1MHz	50ps	-20dBc	4MHz

Table 6-6 : Test bench application summary

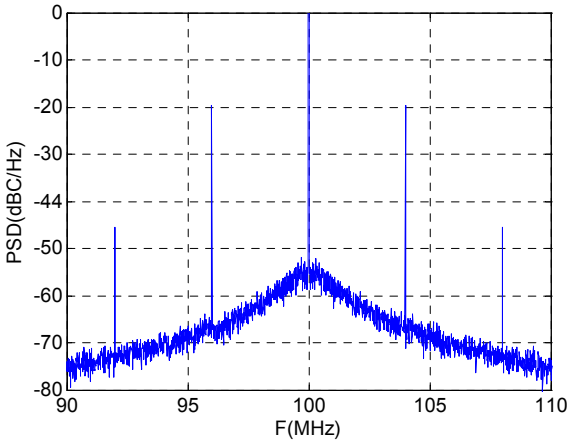


Figure 6-20 : The simulated PLL/DLL spectrum

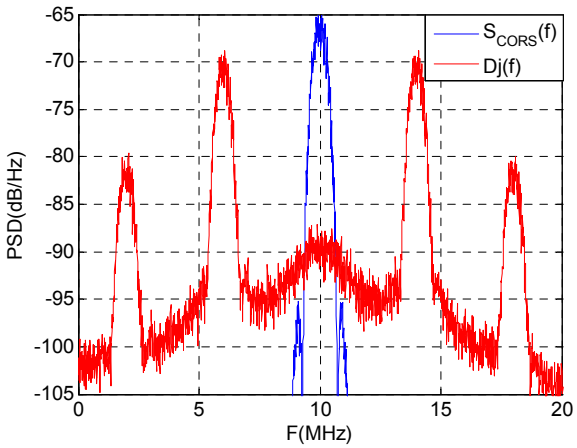


Figure 6-21 : The sampled PSD

The addition of the spurs increases the jitter variance to σ_{rms}=237ps. Figure 6-21 illustrates the jitter distortion and the signal of interest after sampling using the numerical method. The PSD of jitter distortion spectrum contains replicas of the sampled signal by multiples of f_{ref}. As stated in equation (6-5) and verified in the case studies, the jitter distortion is dependent on the signal center frequency. The ratio between $S_{CORS}(f)$ and the replicas on Dj(f) (Figure 6-21) is increased by $(f_0/fs)^2$ in comparison with Δ_{spur}. The jitter distortion inside the band of interest remains unchanged and the SDjR remains the same derived in Figure 6-15, SDjR=20.3dB.

On the following, we add an interferer at the input where the distance in frequency is equal to f_{ref}, (Δf=4MHz from Figure 6-20). The result of the sampled signals is illustrated in Figure 6-22. The interferer falls into an IF=14MHz, and its replica falls inside the band of interest. The interferer–to-signal power ratio of interest is Δ_p=14dB, the Dj(f) of Figure 6-22 gives a SDjR=-9.37dB.

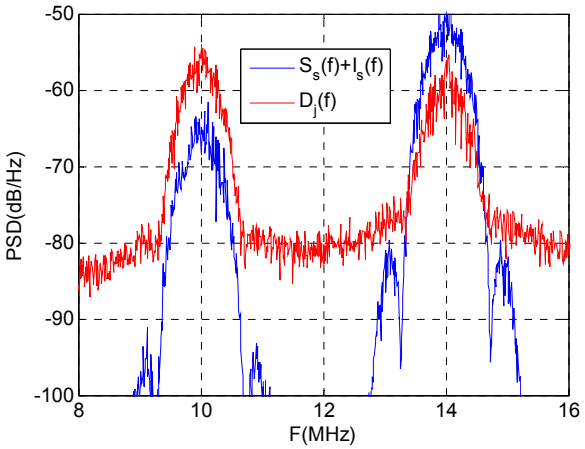


Figure 6-22 : The BPS PSD in presence of phase noise, spurs and an interferer

From Figure 6-20 and Figure 6-21, we observe that the power for the interferer replica is given by $P_{rep}(f)=P_I(f)\cdot\Delta_{spur}\cdot(f_I/fs)^2$ (APPENDIX J). Considering that Dj(f) in the band of interest (around IF=10MHz) is mostly a replica of the interferer $Dj(f)=P_{rep}(f)$ (the case in Figure 6-22), the SDjR is derived:

$$Dj(f)=P_I(f)\cdot\Delta_{spurs}\cdot\left(\frac{f_I}{fs}\right)^2=P_I(f)\cdot\Delta_{spurs\_fI} \tag{6-48}$$

$$SDjR=\frac{P_S}{Dj}=\frac{1}{\Delta_p\cdot\Delta_{spurs\_fI}} \tag{6-49}$$

In this case, the same $(f_I/fs)^2$ ratio is observed. In the BPS process as it is for the mixing process, the spur becomes the most constraining point for the phase noise specifications when $\Delta f=f_{ref.}$ The choice of the reference frequency is closely related to the frequency and the PLL/DLL topology (ex: fractional PLL/DLL). If possible, it is preferable to apply $f_{ref}\neq\Delta f$ in order to relax spurs specifications.

5 Application of the Phase Noise Analysis to the System Level Scaling

In the different test benches carried out previously, SDjR has been defined. In this section the frequency synthesis specifications will be derived for the BT-LE and IEEE802.15.4 standards (Chapter 3). We remind the context where the BPS process is applied. We derive the phase noise specifications for the architecture in Chapter 4 while applying the numerical method and the results from the previous sections.

5.1 Review on the Reference Architecture and the Block to Evaluate Phase Noise

The targeted architecture, illustrated in Figure 6-23, is presented in Chapter 4 [143]. In order to define the blocks specifications for this architecture, the receiver has been spit into building blocks, from B1 to B5. Through application of the proposed method, we define the phase noise specifications for the sampler B3:

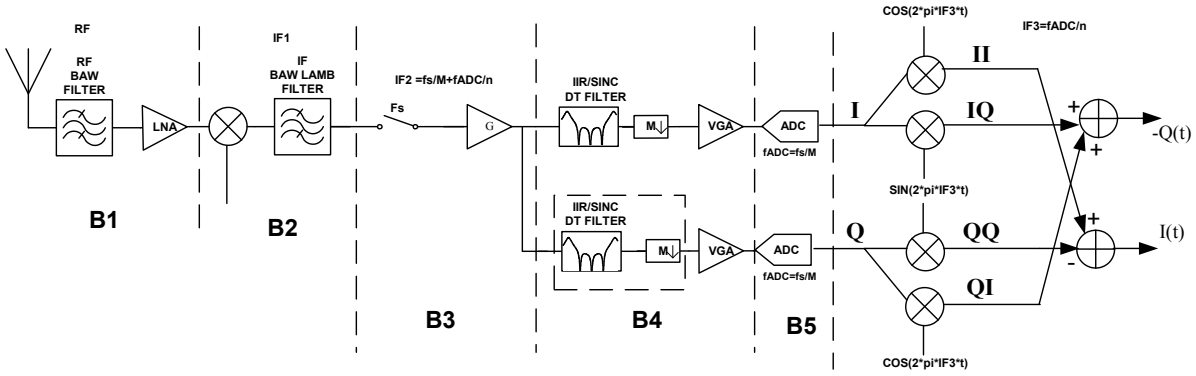


Figure 6-23 : The proposed BPS architecture containing high f_{IF1} and f_{IF1} analog filter

The RF signal is down-converted to a first IF f_{IF1}. The high-IF leads to low-frequency LO for the mixing process, thus relaxing the phase noise constraints for the first down-conversion. As explained in section 2.1, this is the case in the mixing process since the phase noise impact depends only on the LO center.

In Figure 6-23, the accurate sampling frequency for B3 is fs=98MHz. This block samples the signal centered at f_0=IF1=1990.6MHz. As illustrated in Figure 6-23, the signal is down-converted to a second IF IF2=31.2MHz on the BPS process. The frequency plan developed for the proposed architecture is detailed in Chapter 4 and is based on reducing the frequency and on simplifying the filtering techniques.

The system level specification for BT-LE and IEEE802.15.4 for the proposed architecture is detailed in Chapter 4. On the following, the specifications for the block B3 are detailed, in order to define the allowed SDjR on the sampling process, and consequently, the phase noise specifications for this operation. We remind for the sensitivity test bench, the SNR degradation and Gain per block from Chapter 4:

Standard	Parameter	B1	B2	B3	B4	B5	TOTAL
BlueTooth Low Energy	Gv (dB)	10	0	10	28	0	48
	SNR_{deg}(dB)	11.7	4.7	5	1.9	5.7	29
IEEE802.15.4	Gv (dB)	10	6	10	34	0	60
	SNR_{deg}(dB)	11.2	4.5	3.2	0.9	1.7	21.5

Table 6-7 : Summary of the block specifications for the architecture in Figure 6-23

5.2 Defining Specifications on Phase Noise for BT-LE and IEEE802.15.4 on the Proposed Architecture

5.2.1 SDjR Definition in the Presence of an Interferer - L(Δf) and Δ_{spur} specifications

In order to define the SDjR requirements, we take the ULP RF standards specifications presented in Chapter 3 as reference. In the presence of an interferer, the desired signal of interest P_{ds} is set 3dB over the sensitivity level P_{sen} (Figure 6-25). In a test bench in presence of an interferer, a possible distortion (aliasing, reciprocal mixing, intermodulation, and jitter distortion) can be as high as the thermal noise floor P_{n_floor}. The total distortion D_{tot} is increased in 3dB, and the required SNDR is still respected.

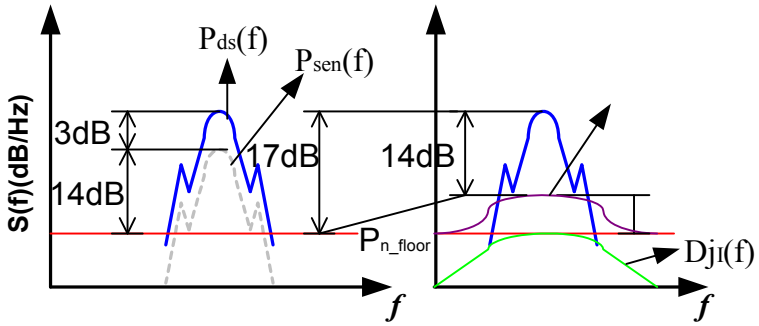


Figure 6-24 : The total distortion in presence of interferer

Table 6-8 summarizes the required specifications on the SDjR:

Standard	Parameter	Value
BlueTooth Low Energy	SNDR	14dB
	SDjR	17dB
IEEE802.15.4	SNDR	3.5dB
	SDjR	6.5dB

Table 6-8 : Summary for the SDjR specifications in the presence of an interferer

The following test bench is used for the numerical method:

$$f_0 = IF1 = 1990.625MHz$$
$$f_s = 98MHz$$

We remind the interferers profile presented in Chapter 3. Table 6-9 summarizes the test benches in terms of Δ_p and Δf. The desired signal level is P_{ds}=-67dBm for BT-LE and P_{ds}=-82dBm for IEEE802.15.4.

Δf	P_{INT_BLE}	Δ_p	$P_{INT\_802.15.4}$	Δ_p
1MHz	-82dBm	-15dB	-	-
2MHz	-50dBm	17dB	-	-
3MHz	-40dBm	27dB	-	-
5MHz	-40dBm	27dB	-82dBm	0dB
10MHz	-40dBm	27dB	-52dBm	30dB

Table 6-9 : Signal levels for the phase noise analysis test bench

The equation of (6-45) is used to set the first values for phase noise specifications. As observed in (6-45), the phase noise specification is referred to the interferer center frequency $L_{fl}(\Delta f)$. Through (6-34), "c" is calculated considering that $\Delta f > fn$, where $|H(f)| \approx 1$. Table 6-10 summarizes the "c" parameter specifications.

Δf	$L_{fl}(\Delta f)_{BLE}$	c	$L_{fl}(\Delta f)_{802.15.4}$	c
1MHz	-62.7dBc	$1.3x10^{-13}$	-	
2MHz	-94.97dBc	$3.2x10^{-16}$	-	
3MHz	-104.97dBc	$7.22x10^{-17}$	-	
5MHz	-104.97dBc	$1.99x10^{-16}$	-70.4dBc	$5.72x10^{-13}$
10MHz	-104.97dBc	$7.96x10^{-16}$	-100.4dBc	$2.28x10^{-15}$

Table 6-10 : Signal levels for the phase noise analysis test bench

The lowest calculated "c" denotes the worst case for the phase noise, which is for Δf=3MHz, therefore $c=7.22X10^{-17}$. From the calculated "c" value, we generate the corresponding jitter distribution on the numerical method. The simulated SDjR is 18.4dB for BT-LE. While applying the numerical method, successive simulations sets the precise value for "c" value required to achieve SDjR=17dB. The resulting "c" is $c=9.78X10^{-17}$, therefore $L_{fl}(\Delta f)$ @ 3MHz=-103.65dBc.

Then, the spurious are added on the phase noise. A first approximation is obtained from (6-49). Applying the numerical method, for SDjR=17dB and Δf=1,2,3MHz for the BT-LE the required spur level referred to f_I are summarized on Table 6-11:

Δf	Δ_{spur_fl}
1MHz	-19dBc
2MHz	-34dBc
3MHz	-45dBc

Table 6-11 : Spur specifications summary for BT-LE

The impacts of $1/f^2$ phase noise behavior and of the spur level Δ_{spur} on the SDjR are summed. The SDjR is fixed to SDjR=17dB for BT-LE and the contributions on the SDjR from $L_{fl}(\Delta f)$ and Δ_{spur_fl} vary from 20% to 80% (Figure 6-25 to Figure 6-27). The spur contribution on the SDjR is indicated on the top X axis and the spur level on the right Y axis. $L_{fl}(\Delta f)$ contribution on the SDjR is indicated on the bottom and the level on the left. On the following results the $L_{fl}(\Delta f)$ is specified for Δf=3MHz and the spurs are specified for different possible f_{ref}=1, 2 and 3MHz.

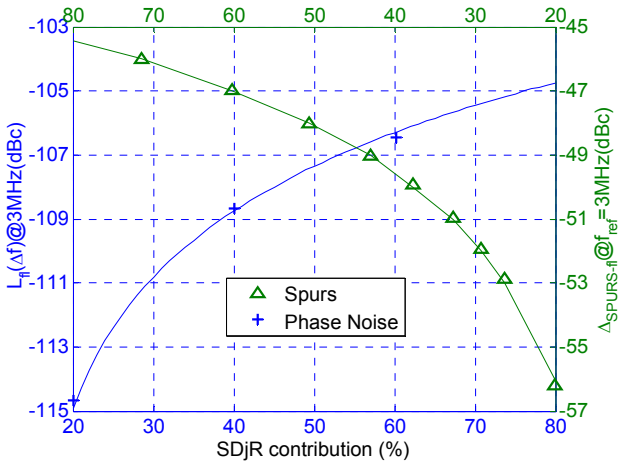


Figure 6-25 : Phase noise specifications and spurs for f_{ref}=3MHz specifications for B3 (Figure 6-23) for BT-LE

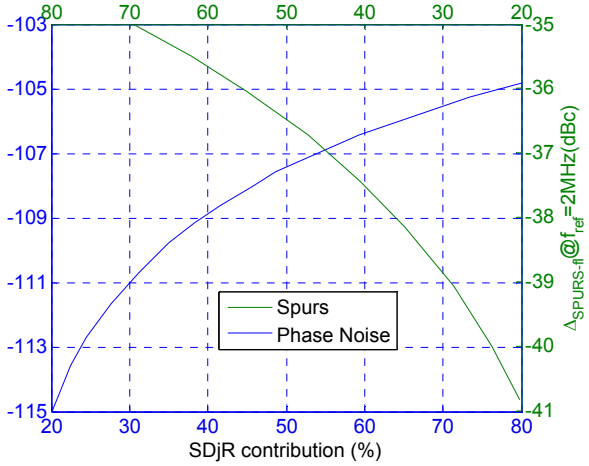


Figure 6-26 : Phase noise specifications and spurs for f_{ref}=2MHz specifications for B3 (Figure 6-23) for BT-LE

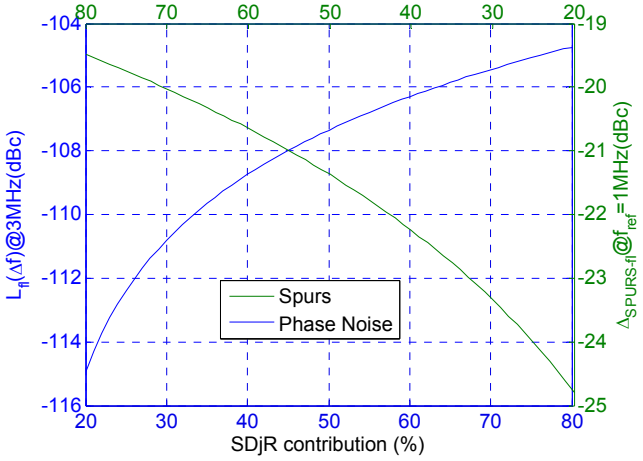


Figure 6-27 : Phase noise specifications and spurs for f_{ref}=1MHz specifications for B3 (Figure 6-23) for BT-LE

The same test benches are applied for the IEEE802.15.4 standard. The results are illustrated in Figure 6-29 and Figure 6-28. The reference SDjR is SDjR=6.5dB. The phase noise specifications are defined for Δf=10MHz, and the spurs considering f_{ref}=5MHz and 10MHz:

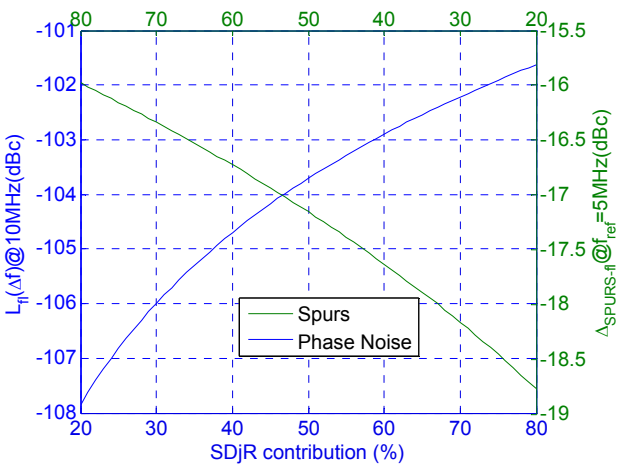


Figure 6-28 : Phase noise specifications and spurs for f_{ref}=5MHz specifications for B3 (Figure 6-23) for IEEE802.15.4

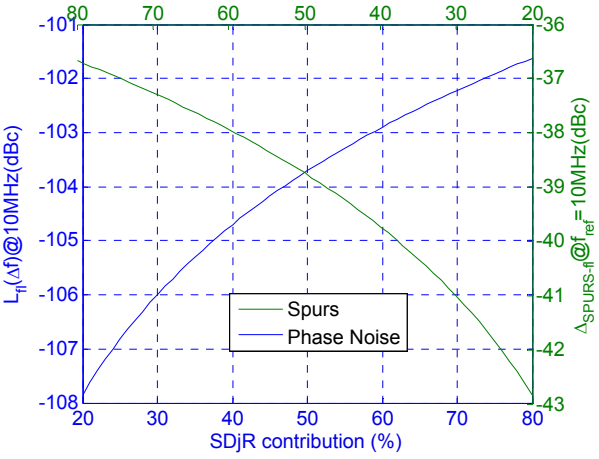


Figure 6-29 : Phase noise specifications and spurs for f_{ref}=10MHz specifications for B3 (Figure 6-23) for IEEE802.15.4

The SDjR in all test cases are dependent on the signal to be sampled center frequency, which is detailed in (6-34), (6-36), (6-41) and (6-49). This is the main difference between the sampling and the mixing process, where the phase noise is referred to the sampling frequency fs and not to the signal center frequency. Yet, the SDjR is dependent on the σ_{rms}. In order to calculate the phase noise specifications referred to fs, the demonstration of APPENDIX J is applied:

$$L_{fs}(\Delta f)=\left(\frac{fs}{f_I}\right)^2 L_{fI}(\Delta f) \tag{6-50}$$

where f_I=IF1+Δf. All the results presented from Figure 6-25 to Figure 6-29 are referred to IF1=1990.625MHz (Figure 6-23).

The results from Figure 6-25 to Figure 6-29 indicates the trade-off between the spur amplitude and phase noise on BPS in presence of interferer. On the implementation level, $L_{fI}(\Delta f)$ and Δ_{spur_fI}. are both dependent on the PLL/DLL order and the cut-off frequency of the loop filter, f_n. For the spur, the PLL/DLL loop filter H(f) behaves as a low-pass filter, so the lower f_n, the stronger the spur is attenuated. On the other hand for $L_{fI}(\Delta f)$, H(f) behaves as a high-pass filter, which impacts the close-to-carrier phase noise where high f_n attenuates it.

In the next section we define the phase noise specifications on the sensitivity case, which is dependent on the close-to-carrier phase noise as it was observed in section 4.1. Since $L_{fI}(\Delta f)$ is specified, we define f_n specifications.

5.2.2 SDjR Definition for the Sensitivity Case – Specifications for f_n Phase Noise Floor

The SDjR specification for the sensitivity case is used to define the close to carrier phase noise. From the presented method in Chapter 3, the blocks are specified in terms of SNR degradation. We remind the chain modeling of the method (Figure 6-30). To consider BPS process, in between two blocks, the aliasing ratio is defined.

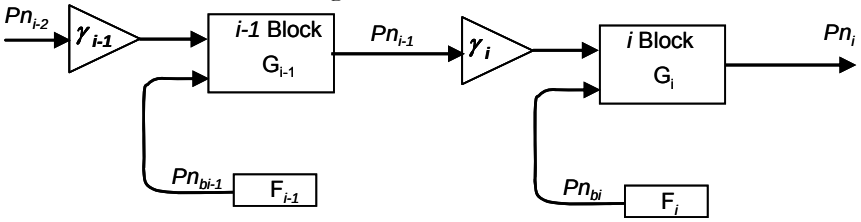


Figure 6-30 : System noise and distortion path block diagram

Pn_i is the input noise. Pnb_i is the input referred generated thermal noise on the i^{th} block.. The SNR_{deg} is the contribution of Pnb and γ_i. Figure 6-31 shows the block diagram where the jitter distortion Dj_i is added as source of SNR degradation, referred to the input:

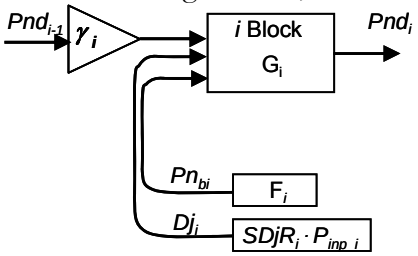


Figure 6-31 : System noise, distortion and jitter error path block diagram

Based on the method described in Chapter 3 we derived the allowed generated input referred error $ERRb_i$, which is a sum of the noise and jitter distortion on the input:

$$ERRb_i = Pn_{i-1} \cdot \left(SNR_{\deg i} - \gamma_i\right) \tag{6-51}$$

$$ERRb_i = Pnb_i + Dj_i \tag{6-52}$$

The jitter error depends on the signal input P_{in} (in V^2):

$$Dj_i = SDjR_i \cdot P_{in\_i} \tag{6-53}$$

Considering the P_{sen} sensitivity level at the antenna amplified by the blocks B1…B5. The input signal at the sampler level B3 is defined as:

$$P_i = P_{sen} \cdot Z_{ant} \cdot G_{B1} \cdot G_{B2} \tag{6-54}$$

Considering the gain and SNR_{deg} budgets defined in Chapter 4 (Table 4-13) and from the simulated aliasing ratio on B3 of Figure 6-23 γ_S =1.7, the allowed input referred error (in V^2) is calculated for both standards:

$$\begin{aligned} ERRb_{s\_BLE} &= -66.2dBmV^2 \\ ERRb_{s\_802.15.4} &= -63dBmV^2 \end{aligned} \tag{6-55}$$

As defined in (6-52), this result is the sum of the jitter distortion and thermal noise contributions. We define the thermal noise for the B3 in order to isolate the allowed jitter distortion. In Chapter 2, the output thermal noise PSD has been defined, which is integrated on the band of interest BW_{CH} for the sample-and-hold noise:

$$P_{n\_S/H,BW_{CH}} = \frac{kT}{C_S}\frac{2}{f_S}BW_{ch}\left(V^2\right) \tag{6-56}$$

where: C_s=sampling capacitance, k=Boltzmann Constant, T=temperature in Kelvin, f_s the sampling frequency.

The sampling capacitor is limited by the block bandwidth, since the signal centered at IF1 should not be filtered by this capacitor. The input signal of interest is centered at IF1=1990.6 MHz. From the system level analysis (Chapter 4), the required sampling capacitor is C_s=800pF. The sampling frequency is fs=98MHz, and the generated thermal noise is given by:

$$\begin{aligned} P_{n\_S/H,BW_{CH},B-LE} &= -68.8dBmV^2 \\ P_{n\_S/H,BW_{CH},802.15.4} &= -65.9dBmV^2 \end{aligned}$$

Therefore, the allowed jitter distortion is (6-52):

$$\begin{aligned} Dj_{s\_BLE} &= -69.4dBmV^2 \\ Dj_{s\_802.15.4} &= -72.85dBmV^2 \end{aligned}$$

From (6-54), P_i (in V^2) at the sampler input is derived. These values are derived from the standards sensitivity input power (Chapter 1), for Z_{ant}=50Ω:

$$\begin{aligned} P_{in\_s\_BLE} &= -46dBmV^2 \\ Pn_{bs\_802.15.4} &= -55dBmV^2 \end{aligned}$$

Applying (6-53), table summarizes the required SDjR:

$SDjR_{s\_BLE} = 23.6dB$
$SDjR_{s\_802.15.4} = 11.2dB$

Table 6-12 : SDjR specifications summary for sensitivity test bench

The expression relating SDjR for the signal of interest and the synthesis jitter is derived in (6-42). Three factors set the value of SDjR : σ_{rms}, f_0 and f_n/BW_{CH}. $L_{fl}(\Delta f)$ is already identified on the test bench in presence of interferer. From (6-34), (6-36) and (6-41) we can link σ_{rms} to $L_{fl}(\Delta f)$:

$$\sigma_{rms,fl}^{\ 2} = \frac{L_{fl}(\Delta f)\cdot \Delta f^2}{2\pi f_n \cdot f_I^{\ 2}} \tag{6-57}$$

The expression (6-57) is applied in (6-42) to define the required SDjR:

$$10\log(SDjR) = -10\log\left(\frac{L_{fl}(\Delta f)\cdot \Delta f^2}{2\pi f_n}\right) + \theta\frac{f_n}{BW_{CH}} + \beta \tag{6-58}$$

$\theta = 5.09 \qquad \beta = -16.08$

From (6-58) we can derive the f_n for each value of $L_{fl}(\Delta f)$ from Figure 6-25 to Figure 6-29 in order to respect the SDjR of Table 6-11. From the first calculation, successive simulations using the numerical method are applied.

Figure 6-32 illustrates the minimum required f_n for a given $L_{fl}(\Delta f)$ obtained from Figure 6-25 Figure 6-27 for BT-LE. Figure 6-33 illustrates the minimum required f_n for a given $L_{fl}(\Delta f)$ obtained from Figure 6-28 and Figure 6-29 for IEEE802.15.4:

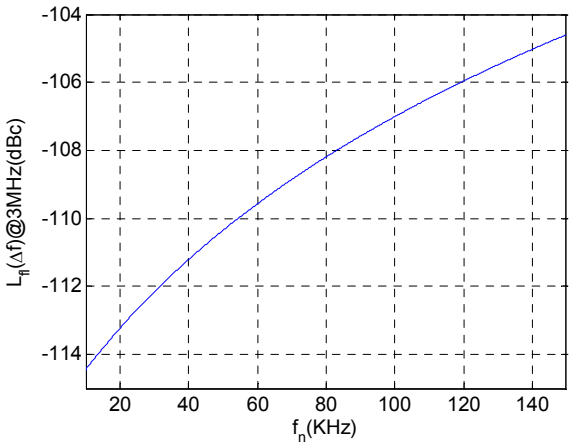


Figure 6-32 : f_n vs $L_{fl}(\Delta f)$ @3MHz for BT-LE specifications

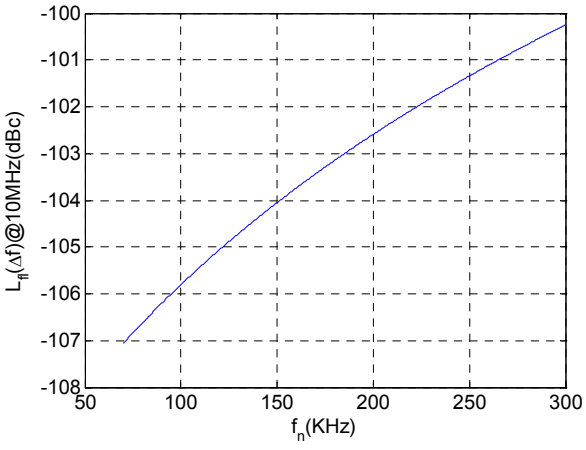


Figure 6-33 : f_n vs $L_{fl}(\Delta f)$ @10MHz for IEEE802.15.4 specifications

The last parameter to consider is the phase noise floor. As it has been defined in equation (6-21), the SDjR from BPS process is defined considering fs=98MHz and IF1=1990.6MHz. The required SDjR is defined in Table 6-12. From a given required σ_{AP}, the phase noise floor is calculated as follows:

$$PSD_{n\_floor}(dBc/Hz) = \sigma_{AP}^{\ 2}\frac{2}{BW_{noisef}} \tag{6-59}$$

The white phase noise floor is defined for a given noise bandwidth BW_{noise}, which is dependent on the sampler cut-off frequency in our application. The SDjR from Table 6-12 is used as reference. As we have separated the contributions between $L_{fl}(\Delta f)$ and Δ_{spurs_fI} in the presence of interferers test bench, we separate in this section the contributions from the white phase noise floor and the synthesis phase noise on the SDjR for the sensitivity case test bench. The required σ_{AP} is computed through (6-20) and summarized in Figure 6-34 for BT-LE and in Figure 6-35 for IEEE802.15.4. The required phase noise floor is computed through (6-59). Finally, the specifications of f_n given in Figure 6-32 and Figure 6-33 consider that the close-to-carrier $L_{fl}(\Delta f)$ contributes with 100% of the SDjR on the sensitivity case. Since the contributions on SDjR from σ_{AP} and $L_{fl}(\Delta f)$ are complementary, the specifications of f_n vs $L_{fl}(\Delta f)$ are recomputed for contributions of 20%, 50% and 70% on the SDjR. The results are summarized in Figure 6-36 and Figure 6-37.

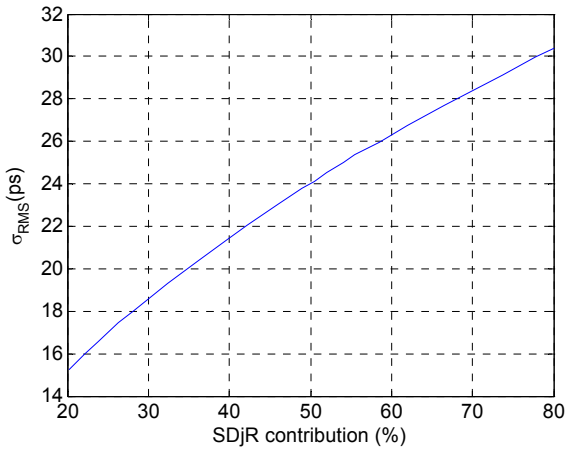


Figure 6-34 : σ_{RMS} vs SDjR contribution of phase noise floor for BT-LE

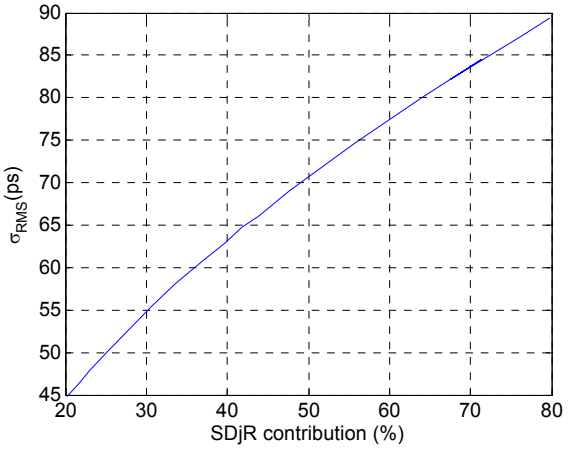


Figure 6-35 : σ_{RMS} vs SDjR contribution of phase noise floor for IEEE802.15.4

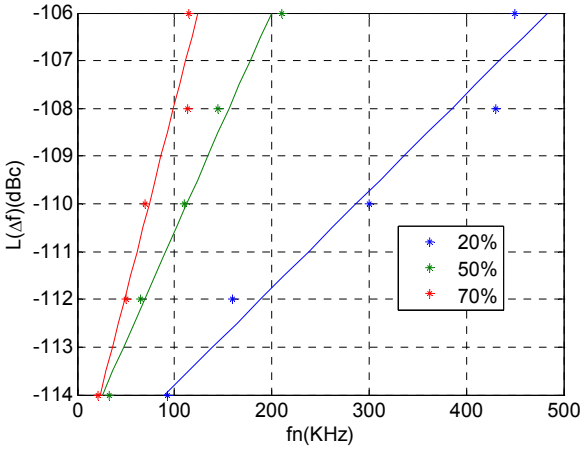


Figure 6-36 *fn* vs L(Δf) @3MHz for BT-LE specifications

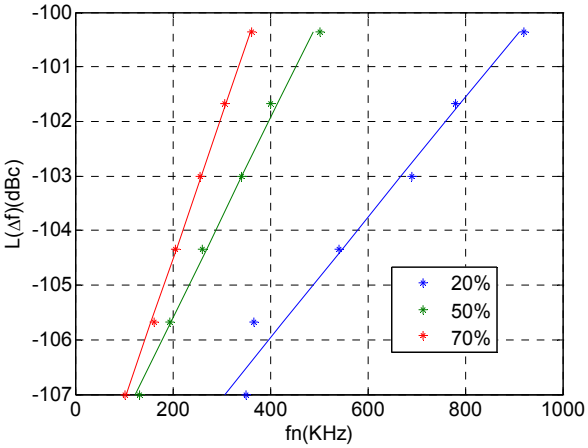


Figure 6-37 : *fn* vs L(Δf) @3MHz for IEEE802.15.4 specifications

Finally, we present a numerical example in order to explain how to read the phase noise specifications through the illustrated results.

We consider the BT-LE for this numerical example. First, we observe the spurious position dependent on the reference frequency. Consider the case of Figure 6-25 where the spur

is at f_{ref}=3MHz. If the spur amplitude is Δ_{spur_fl}=-47dBc, it contributes to 60% of the required SDjR, the other 40% is obtained from Figure 6-25 for a $L_{fl}(\Delta f)$ @ Δf =3MHz, which is $L_{fl}(\Delta f)$=-108.7dBc. For the sensitivity test bench, $L_{fl}(\Delta f)$=-108.7dBc lead to f_n=75KHz, which is derived in Figure 6-32. Now consider an aperture jitter of σ_{AP}=24 ps, we observe from Figure 6-34 that it represents 50% of the contribution on the SDjR derived in Table 6-12. In this case, f_n is updated in order to consider the white phase noise floor, the phase noise from the synthesis jitter contributes with the other 50%, which is the green line of Figure 6-36, and for $L_{fl}(\Delta f)$=-108.7dBc it leads to f_n=150KHz.

5.3 Impact on the Power Consumption of the Phase Noise Specifications for Bandpass Sampling

In the previous sections, we derived the phase noise specifications for the proposed architecture of Chapter 4. The architecture is based on reducing the power consumption of the block by reducing the frequency of synthesizer block. The objective of this Chapter is first to define the phase noise specifications in the context of BPS and to analyze if the resulting specifications represent an increase or decrease on the power consumption of the frequency synthesis blocks.

In Chapter 2, a state of the art considering the last developments on PLL/DLL low power oriented has been done. The following FoM for the VCO has been derived:

$$FoM = \left(\frac{f_0}{\Delta f}\right)^2 \cdot \frac{1}{\left(L(\Delta f)\cdot P\right)} \tag{6-60}$$

We observe from (6-60) that for constant FoM and power, the phase noise increases with the square of the center frequency, following the same trend presented in APPENDIX J . What is observed in the derived equations for the SDjR, is that it is dependent on the process variance, therefore on the $L(\Delta f)/f_0^2$ ratio (6-57). If $L(\Delta f)/f_0^2$ is kept constant even for different f_0 it leads to the same power consumption at constant FoM.

As a sum-up, if lower fs are used, lower $L_{fl}(\Delta f)$ are specified, but for constant FoM, it leads to constant power. The first study in Chapter 2 has been to verify if for different center frequencies for the oscillator, the FoM is kept. Interestingly, the FoM increased for lower frequencies, for example f_{LO}=400MHz [58] and f_{LO}=641MHz [52] (see details in Chapter 2), which actually leads to very low power consumption considering the achieved FoM. The specifications on the previous sections are referred to IF1. Considering fs=98MHz, we analyze the synthesis phase noise specifications referred to fs in the case the spurs are @ f_{ref}=1MHz (Figure 6-38). Now considering the FoM_{dB}=195.2dB of [58] $L_{fs}(\Delta f)$@3MHz of $L_{fs}(\Delta f)$=-133.3dBc, when the Δ_{SPUR_fs}=-47.4dBc (50% 50% to the SDjR). The estimated power consumption (6-60) is P_{VCO}=700μW.

For PLL frequency synthesizer, power estimations are discussed in [144], where the most critical building blocks, which consume quiescent current, are the *Multi-Modulus frequency Divider* (MMD) and the charge pump *Phase-Frequency Detector* (PFD), where the power can be estimated as follows:

$$P_{pll} = b_1 \cdot C_1 \cdot V_{dd}{}^2 \cdot f_{LO} + b_2 \cdot C_2 \cdot V_{dd}{}^2 \cdot f_{ref} \quad (6\text{-}61)$$

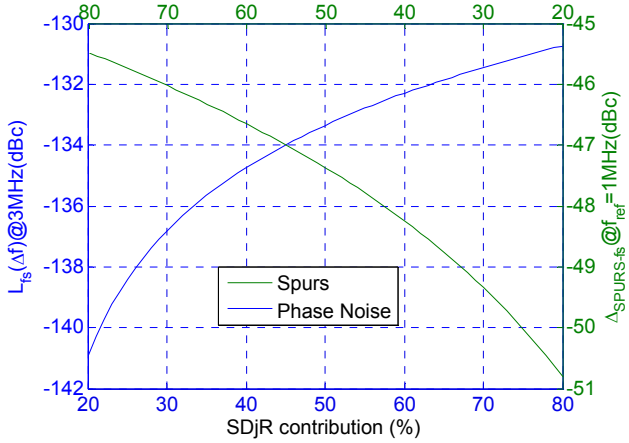


Figure 6-38 : Phase noise specifications and spurs for f_{ref}=3MHz specifications for B3 (Figure 6-23) for BT-LE

C_1 and C_2 represent the total parasitic capacitance loading the RF blocks, and V_{dd} the supply voltage. The first term b_1 of the equation is associated with the power consumption of the frequency divider as well as the buffers working at f_{LO} frequency. The second term b_2 is a proportionality constant which includes the process, the reference buffers and the charge pump PFD.

It was observed that the power requirement for the oscillator does not change for a given specification when lower f_{LO} is applied, since $L(\Delta f)/f_0^2$ ratio is kept constant. Consider that b_1 b_2 C_1 C_2 and f_{ref} are kept constant. In a classical mixing process, $f_{LO}=f_0$ to down-convert the signal to base band, where in BPS fs can be decreased up to a bottom limit where $fs<<f_0$. In our example of Figure 6-23, the highest needed frequency for f_{LO} is around 480MHz, which means a PLL power economy of 5 times for the buffers and the frequency divider (first term on (6-61)).

In conclusion the lower f_{LO} applied on the PLL does not impact the power consumption on the oscillator level, since $L(\Delta f)/f_0^2$ is kept constant. Finally, the f_{LO} reduction represents proportional power saving on the output buffer levels.

6 Conclusions

In the objective to evaluate and specify the jitter / phase noise requirements on the BPS process, a new numerical method is presented and validated. An analytical approach is first developed and compared with the proposed numerical method. Whenever a correlated jitter is applied, the jitter distortion is concentrated around the sampled signal of interest. The SDjR is not dependent on the under-sampling ratio in this case. This is a non-intuitive conclusion and is different from non-correlated jitter. On Table 6-13 we summarize the relations, some of them semi-empirical, for the SDjR in the different cases.

We observed that the most constraining test bench consists in the presence of interferer where intermodulation occurs on the $1/f^2$ phase noise and spurs levels. The phase noise

specifications are referred to IF1 and the distance where the phase noise is more constraining is 3MHz for BlueTooth Low Energy and 10MHz for IEEE802.15.4

Jitter / Test Bench Type	**Expression**
Aperture Jitter / Sensitivity	$SDjR = \frac{1}{2\cdot(2\pi)^2\sigma^2 f_0^{\,2}}\frac{fs}{BW_{CH}}$
Synthesis Jitter / Sensitivity	$10\log(SDjR) = -20\log(\sigma_{rms} f_0) + \theta\frac{f_n}{BW_{CH}} + \beta$ $\theta = 5.09 \qquad \beta = -16.08$
Synthesis Jitter / Presence of Interferer	$10\log(SDjR) = 10\log\left(\frac{1}{L_{fl}(\Delta f)}\cdot\frac{1}{\Delta_p}\right)\cdot\theta + \beta$ $\theta = 0.88 \qquad \beta = -50.28$
Spurs Phase Noise / Presence of Interferer	$SDjR = \frac{P_S}{Dj} = \frac{1}{\Delta_p\cdot\Delta_{spurs\_fl}}$

Table 6-13 : Summary for the SDjR expressions

For different possible reference frequencies f_{ref}=1, 2, 3, 4, 5 and 10MHz, the spurious specifications are derived. The trade-off between phase noise and spurs power appear in Figure 6-25 to Figure 6-29 for the proposed architecture of Chapter 4. The specifications are given in terms of graphics to give more design margin, considering different possible configurations between the phase noise and the spur specifications.

The last two specifications of the phase noise, which are the cut-off frequency f_n and the phase noise floor, are both dependent on the phase noise specified from Figure 6-25 to Figure 6-29. In this case the applied test bench is the sensitivity case. Figure 6-32 to Figure 6-37 defines the trade-off between synthesis jitter and aperture jitter for the defined specifications.

The interest of applying low f_{LO} on the BPS process is presented in section 5.3. From (6-60) For the VCO, whenever the $L(\Delta f)/f_0^2$ ratio is kept constant, the VCO power consumption is unchanged for constant FoM. What is observed in the state of the art is an increase on the FoM for lower frequencies. In addition, decreasing f_{LO} reduces the output buffer power consumption. We can therefore conclude that the proposed architecture of Chapter 4, represent a very interesting configuration in terms of power consumption, since the frequency plan is design in order to strongly reduce the synthesizer frequencies.

APPENDIX G - THE DERIVATION FOR THE POWER SPECTRAL DENSITY OF A SEQUENCE OF AN NON-UNIFORMLY DISTRIBUTED DIRAC PULSES

In order to derive G(f) [135], we define g(t) as a random process, which PSD is by definition the Fourier Transform of the autocorrelation function of g(t) :

$$G(f)=\int_{-\infty}^{\infty} R_g(\tau)e^{-j2\pi f\tau}d\tau \tag{6-62}$$

where $R_g(\tau)$is the autocorrelation function expressed by:

$$R_g(\tau)\equiv E(g(t)g(t-\tau)) \tag{6-63}$$

Let's consider $X_T(f)$ as the truncated Fourier Transform of the random process g(t) defined as:

$$X_T(f)\equiv\int_0^T g(t)e^{-j2\pi ft}dt \tag{6-64}$$

The PSD is therefore defined as:

$$G(f)=\lim_{T\to\infty}\frac{E|X_T(f)|^2}{T} \tag{6-65}$$

where the quantity $S_T(f)=\frac{E|X_T(f)|^2}{T}$ is known as the *periodogram*

When applying the periodogram as a statistical estimator of the DSP the longer the observed interval T, the better the estimation resolution. In any case, with $T\to\infty$, we obtain the exact PSD (6-65). In this derivation, we first define $X_T(f)$, then the periodogram is calculated as a function of T. When the probability density function is known, the exact statistical expectation of $X_T(f)$ can be computed. We remind g(t) defined in section 2.3:

$$g(t)=\sum_{n=-\infty}^{\infty}\delta(t-nTs-\Delta_n) \tag{6-66}$$

We define the truncated Fourier Transform of (6-66), observed in a time interval of T=KTs, K integer:

$$X_{KT_S}(f)\equiv\int_0^{KTs}\sum_{n=0}^{K-1}\delta(t-nTs-\Delta_n)e^{-j2\pi ft}dt=\sum_{n=0}^{K-1}e^{-j2\pi f(nTs+\Delta_n)}dt \tag{6-67}$$

leading to:

$$E|G_{KT_S}(f)|^2=E\left|\sum_{n=0}^{K-1}e^{-j2\pi f(nT+\Delta n)}\right|^2=\sum_{n,m=0}^{K-1}e^{-j2\pi f(n-m)Ts}E(e^{-j2\pi f(\Delta n-\Delta m)}) \tag{6-68}$$

Considering that Δ_n and Δ_m as independent random processes; the expectation above is therefore defined by:

For n=m, $E(e^{-j2\pi f(\Delta n-\Delta m)})=1$ (6-69)

For n≠m, $E(e^{-j2\pi f(\Delta n-\Delta m)})=W(f)=\int_{-\infty}^{\infty}f(\Delta n)d\Delta n\int_{-\infty}^{\infty}f(\Delta m)d\Delta m\,e^{-j2\pi f(\Delta n-\Delta m)}$ (6-70)

W(f), is the cross correlation of the processes Δ_n and Δ_m., $f(\Delta_n)$ and $f(\Delta_m)$ are respectively the probability density functions for Δ_n and Δ_m. respectively. Combining (6-69) and (6-70) equations on (6-68) and after simplification, we obtain:

$$E\left|G_{KT_s}(f)\right|^2 = W(f)\left(\frac{\sin(\pi f K T_s)}{\sin \pi f T_s}\right)^2 + K(1-W(f)) \tag{6-71}$$

Applying this relationship in (6-65), yields:

$$G(f) = \lim_{K\to\infty} \frac{E\left|G_T(f)\right|^2}{KT_s} = \frac{W(f)}{{T_s}^2} \sum_{n=-\infty}^{\infty} \delta\left(f - \frac{n}{T_s}\right) + \frac{1-W(f)}{T_s} \tag{6-72}$$

For our analytical approach, W(f) is calculated for a Gaussian and uniform distributions. For the uniform distribution, the limits [-β;β]are considered and the variance σ^2 for Gaussian distribution :

$$W_{un}(f) = \frac{1}{4\beta^2} \int_{-\beta}^{\beta}\int_{-\beta}^{\beta} e^{-2\pi f(x-y)}dxdy = \sin c^2(2f\beta) \text{ for uniform distribution} \tag{6-73}$$

$$W_{gaus}(f) = \frac{1}{2\pi\sigma^2} \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} e^{-\left(x^2+y^2\right)/2\sigma^2} e^{-2\pi f(x-y)}dxdy = e^{\left(-4\sigma^2\pi^2 f^2\right)} \text{ for Gaussian} \tag{6-74}$$

distribution

The PSD for a sequence of non-uniformly distributed Dirac Pulses is also known on the *Ultra Wide Band* (UWB) radio domain. The spectrum is often classified between the discrete spectrum, called the spectral lines, and a continuous spectrum contribution. Analyzing (6-72) we observe a sequence of spectral lines distanced 1/Ts and attenuated by the weight function *W(f)*, which is dependent on the distribution of Δ_n and Δ_m, defined above. The second term of (6-72) is the continuous spectrum of *G(f)*.

APPENDIX H - THE ANALYTICAL DERIVATION FOR THE BPS SDJR FOR NON-CORRELATED JITTER AND COSINE INPUT SIGNAL

In section 3.1 G(f) has been defined as the PSD of Dirac pulses sequence with period Ts and jitter Δ_n. S(f) was defined as the PSD of the signal of interest to be sampled. The BPS process is defined as the convolution product between these two PSDs:

$$S_S(f) = G(f) * S(f) \tag{6-75}$$

The analytical form for G(f) was derived on the previous appendix:

$$G(f) = \frac{W(f)}{T_s^2} \sum_{n=-\infty}^{\infty} \delta\left(f - \frac{n}{T_s}\right) + \frac{1 - W(f)}{T_s} \tag{6-76}$$

where W(f) was for uniform and Gaussian non-correlated random process distributions:

$$W_{un}(f) = \mathrm{sinc}^2(2f\beta) \text{ for uniform distribution ([-β;β] the interval)} \tag{6-77}$$

$$W_{gans}(f) = e^{\left(-4\sigma^2\pi^2 f^2\right)} \text{ for Gaussian distribution (}\sigma^2\text{ the variance of the process)} \tag{6-78}$$

While applying (6-75) on (6-76), we derive:

$$S_S(f) = S(f) * \left[\frac{W(f)}{T_s^2} \sum_{n=-\infty}^{\infty} \delta\left(f - \frac{n}{T_s}\right)\right] + S(f) * \left[\frac{1 - W(f)}{T_s}\right] \tag{6-79}$$

In order to derive the analytical SDjR for a cosine input we define the analytical form of S(f):

$$S(f) = \frac{A^2}{4}\left[\delta(f - f_0) + \delta(f + f_0)\right] \tag{6-80}$$

The first term on (6-79) is the convolution of the signal of interest by the spectral lines of G(f). The N^{th} harmonic of G(f) spectral line down-converts the signal of interest in the BPS process. This convolution product is the sampled signal of interest $S_{CORS}(f)$:

$$S_{CORS}(f) = \frac{A^2}{4} \frac{W(N/Ts)}{T_S^2} \cdot \left[\delta\left(f - \frac{N}{Ts} - f_0\right) + \delta\left(f - \frac{N}{Ts} + f_0\right)\right] \tag{6-81}$$

The continuous part of the G(f) is considered as phase noise, and the PSD of jitter distortion Dj(f) is defined as the convolution product between the continuous spectrum of G(f) and S(f):

$$Dj(f) = \frac{A^2}{4 \cdot Ts}\left[1 - W(f - f_0) + 1 - W(f + f_0)\right] \tag{6-82}$$

The local SDjR is defined as the ratio between $S_{CORS}(f)$ and Dj(f) integrated between f1 and f2:

$$SDjR(f_1, f_2) = \frac{\int_{f1}^{f2} S_{CORS}(f)df}{\int_{f1}^{f2} Dj(f)df} \tag{6-83}$$

$$SDjR(f_1,f_2)=\frac{1}{T_S}\frac{W(N/T_S)}{\int_{f1}^{f2}[2-W(f-f_0)-W(f+f_0)]df} \tag{6-84}$$

Therefore to analyze the local SDjR in the presence of Gaussian and uniform distributions, (6-77) and (6-78) are applied in (6-84), leading to:

$$SDjR_{uni}(f_1,f_2)=\frac{1}{T_S}\frac{\sin c^2\left(2N/T_S\beta\right)}{\int_{f1}^{f2}[2-\sin c^2(2(f-f_0)\beta)-\sin c^2(2(f+f_0)\beta)]df} \tag{6-85}$$

$$SDjR_{gauss}(f_1,f_2)=\frac{1}{T_S}\frac{e^{\left(-4\sigma^2\pi^2\left(\frac{N}{T_S}\right)^2\right)}}{\int_{f1}^{f2}\left[2-e^{\left(-4\sigma^2\pi^2(f-f_0)^2\right)}-e^{\left(-4\sigma^2\pi^2(f+f_0)^2\right)}\right]df} \tag{6-86}$$

For the uniform distribution β is changed so that the variance of the process appears in the equation:

$$\sigma=\sqrt{\frac{(2\beta)^2}{12}} \tag{6-87}$$

We also need to define f1 and f2 in terms of BW_{CH} (the signal of interest bandwidth) and fs (the sampling frequencies). On the following Figure 6-39, we apply equations (6-85) and (6-86) to illustrate $SNDR{\cdot}BW_{ch}$ / fs vs $(\sigma f_0)^2$:

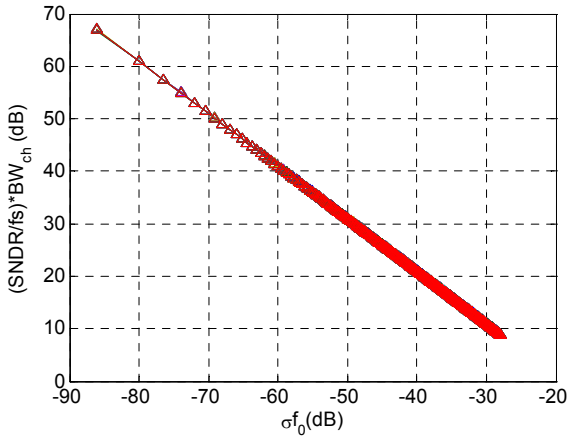


Figure 6-39 : SDjR BW_{ch} / fs X $(\sigma f_0)^2$

To find a simplified version of (6-85) and (6-86) for the linear region visualized in Figure 6-39, a Taylor series expansion approach is applied. Since the curves are superposed in Figure 6-39, only (6-85) will be analyzed. Consider the integral from the bottom part of equation (6-85) developed from 0 to BW_{ch}:

$$\int_0^{BW_{ch}} Dj(f)df=\int_0^{BW_{ch}}[2-\mathrm{sinc}^2(2(f-f_0)\beta)-\mathrm{sinc}^2(2(f+f_0)\beta)]df \tag{6-88}$$

Now the function sinc can be expanded as Taylor Series limited to the second order around the linear region $2(f-f_0)\beta$ and $2(f+f_0)\beta$ =0,01 (the linear region of Figure 6-39). This approach is possible when the interval $(f2+f1)/2 << f_0$. It means that such simplification is valid only when fs<f0, i.e. k >1.

The result for the Taylor series expansion gives:

$$\sin c^2(x)\Big|_{x_0=0.01} = a - b(x - x_0) - c(x - x_0)^2 \tag{6-89}$$

Where:

$$a = 0.999671$$
$$b = 0.06578$$
$$c = 3.28727$$

Applying this result on (6-88) gave:

$$\int_0^{BW_{ch}} Dj(f)df = 2BW_{ch} - \int_0^{BW_{ch}} \left[a - b(2(f - f_0)\beta - 0.01) - c(2(f - f_0)\beta - 0.01)^2\right]df - \int_0^{BW_{ch}} \left[a - b(2(f + f_0)\beta - 0.01) - c(2(f + f_0)\beta - 0.01)^2\right]df \tag{6-90}$$

The integral is given by:

$$\int_0^{BW_{ch}} Dj(f)df = BW_{ch}\left[2X(\beta f_0)^2 + 2Y(\beta BW_{ch})^2 + 2Z\beta BW_{ch}\right] \tag{6-91}$$

Where:

$$X = 13.1491$$
$$Y = 4.38303$$
$$Z = 3.46x10^{-5}$$

From the fact that $BW_{ch} << f_0$ only just the first term of (6-91) is considered. Applying the result of (6-91) in (6-85) the interpolated function is obtained:

$$SDjR(0, BW_{ch}) = \frac{1}{T_S}\frac{\operatorname{sinc}^2\left(2\,N/T_S\,\beta\right)}{BW_{ch}\left[2X(\beta f_0)^2\right]} = \frac{1}{T_S}\frac{1}{BW_{ch}\left[2X(\beta f_0)^2\right]} \tag{6-92}$$

We substitute β for σ (6-92) using the relation of (6-87), which gives:

$$\frac{SDjR(0, BW_{CH})BW_{CH}}{fs} = \frac{1}{6X(\sigma f_0)^2} \tag{6-93}$$

The same expression can be obtained using the calculated points of Figure 6-39 and applying a first order polynomial fit. Since the variable X is defined above, (6-93) becomes:

$$SDjR(0, BW_{CH}) = \frac{1}{78.9 \cdot \sigma^2 f_0^{\,2}}\frac{fs}{BW_{CH}} \tag{6-94}$$

APPENDIX I - THE BPS SDJR FOR NON-CORRELATED JITTER AND COSINE INPUT SIGNAL AND THE PRESENCE OF AN INTERFERER

Another interesting case is studied through analytical development, corresponding to the presence of an interferer in the input. The amplitude of the interferer is $A_I > A_S$ (A_S the signal of interest amplitude) and center frequency f_I.

$$i(t) = A_I \cos(2\pi f_I t) \tag{6-95}$$

While equation (6-81) is kept, equation (6-82) becomes:

$$Dj(f) = \frac{A_I^{\,2}}{4 \cdot Ts}\left[1 - W(f - f_I) + 1 - W(f + f_I)\right] \tag{6-96}$$

We apply (6-96) in the expression (6-83) in order to derive the SDjR in presence of an interferer:

$$SDjR(f_1, f_2) = \frac{\int_{f1}^{f2} S_{S\_\text{int}}(f)df}{\int_{f1}^{f2} Dj(f)df} = \frac{A_S^{\,2}}{A_I^{\,2}} \frac{1}{T_S} \frac{W(k/T_S)}{\int_{f1}^{f2}\left[2 - W(f - f_I) - W(f + f_I)\right]df} \tag{6-97}$$

We apply the same method described in the previous appendix and the expression (6-97) in order to derive the SDjR in presence of interferer:

$$SDjR(0, BW_{ch}) = \frac{A_S^{\,2}}{A_I^{\,2}} \frac{1}{78.9 \cdot \sigma^2 \cdot f_I^{\,2}} \frac{fs}{BW_{CH}} \tag{6-98}$$

APPENDIX J - RELATION BETWEEN THE PHASE NOISE REFERRED TO THE LO AND REFERRED TO THE SIGNAL CENTER FREQUENCY

From expression (6-5), we observe that the jitter distortion is proportion to the signal to be sampled center frequency and process variance. We consider the following phase noise referred to the sampling frequency $L_{fs}(\Delta f)$:

$$L_{fs}(\Delta f) = \frac{\sigma_c^{\,2} \cdot fs^{\,3}}{\Delta f^{\,2}} \cdot \tag{6-99}$$

Where the jitter variance is calculated from (6-41):

$$\sigma_{rms}^{\,2}{}_{,fs} = \frac{\sigma_{c,fs}^{\,2} \cdot fs}{\omega_n} \cdot \tag{6-100}$$

Now we consider the phase noise referred to the signal center frequency f_0:

$$L_{f0}(\Delta f) = \frac{\sigma_{c,f0}^{\,2} \cdot f_0^{\,3}}{\Delta f^{\,2}} \cdot \tag{6-101}$$

We define the same the jitter variance for the phase noises of (6-99) and (6-101):

$$\sigma_{rms}^{\,2}{}_{,f0} = \frac{\sigma_{c,f0}^{\,2} \cdot f_0}{\omega_n} = \frac{\sigma_{c,fs}^{\,2} \cdot fs}{\omega_n} = \sigma_{rms}^{\,2}{}_{,fs} \tag{6-102}$$

We define the relation between $L_{fs}(\Delta f)$ and $L_{f0}(\Delta f)$ applying (6-102) on (6-101) and (6-99):

$$L_{fs}(\Delta f) = \left(\frac{fs}{f_0}\right)^2 L_{f0}(\Delta f) \tag{6-103}$$

Chapter 7 : Conclusion and Perspectives

1 General Conclusions and Results

Two important aspects make DT architectures a very promising technique for to the next generation RF receivers: the continuous developments towards miniaturization of advanced digital-oriented CMOS process and the continuous development towards VLSI process on SoCs. With the required convergence of various digital communication protocols, the nowadays context pushes the need for agile and multi-standard receivers. DT receivers offer such possibility by the means of DT filtering and decimation. In this context, the BPS technique is presented as a solution to reduce the frequency synthesizer constraints on receivers. The objective of thesis is to propose and specify new DT receiver based on Band Pass Sampling processing architecture capable of addressing both characteristics of agile multi-standard and ultra low-power receiver. The five chapters in this document tackles challenges concerning system level design of DT architecture. The objectives are to find gaps in the literature architectures, to define an innovative solution in this context and to give detailed analysis on the highlighted critical blocks.

The first chapter is dedicated on the state of the art. This chapter presents a wide data base related to the thesis key points: The BPS sampling process on DT architectures and ultra low-power receivers. We highlight the challenge of spectral aliasing and filtering/noise trade-off on the voltage and charge sampling techniques related to BPS process. A key issue on these architectures is to define the correct anti-aliasing technique. We classify the DT architectures found in the literature in three distinct families. A comparative table underlines the pros and cons on these architectures. What is generally observed is a major concern on reconfigurability on the detriment of the power consumption. While the frequency plan is rather simplistic, it does not relax filtering and frequency synthesis technique, providing with the first clues for improvement. The state of art on the basic blocks of DT architecture aims at presenting the framework on the block specifications and figure of merits to orient the system level design. A special attention is paid on the frequency synthesis blocks considering their high contribution on the total power consumption and the fact that the BPS can reduce the oscillator frequencies on the receiver.

In classical system level design flow, the work starts from a spread sheet calculation and simulation starts from time domain data flow simulation towards behavioral modeling. The new system level challenges on the BPS process, in particular the different filtering process inherent to the sampling (charge or voltage sampling) and the multiple aliasing on of the wideband input spectrum, motivated the development of the new system level simulation tool. The iterative system design method was developed to optimize the constraints distribution regarding the impact in terms of power consumption. Differently from Friis formula, the method puts into consideration the noise aliasing and the addition of different parasitic sources on the signal distortion. The present simulation tool is also particularly dedicated to take into consideration the BPS process. Presenting hybrid frequency/time domain calculation and frequency domain SNDR evaluation, the tool fulfills a gap on the design flow between the high level models of base band data flow BER simulation, which are far from the implementation level, and the time domain behavioral modeling, which on the other hand are not flexible in terms of simulation time to try and analyze a wide range of configurations. The presented tool brings another two aspects: the different sources of signal distortion are analyzed calculated separately thanks to correlation

calculations based on the Bussgang theorem, and the vector signal processing which can accelerate simulation time while keeping the results precision.

In the objective to analyze in depth the choices of the different DT architectures, we design at system level one configuration per architecture family figured out in the state of the art. The process is speed up using the presented method and simulation tool. While some architectures present high sampling frequencies and filtering order, others are strongly dependent on CT passive filtering. A particular attention is paid on the frequency plan and filtering techniques to present an innovative architecture. The new architecture relies on applying a high first intermediate frequency and high under-sampling ratio. A low-IF frequency is preferred rather than a zero-IF, and for decimation, aliasing rejection and image rejection, a complex DT filter is employed. While it brings the advantage of reducing the frequency synthesis by a ratio of 5, this architecture also reduces the needed DT filter order by a factor of 4, and performances in terms of rejection is maintained. The derived frequency plan makes it possible to apply at the same time IIR functions and a low-IF scheme which reduces the ADC needs in terms of dynamic range (12dB) and relaxes the constraints linked to zero-IF scheme (1/f noise, IIP2 and DC offset). The dynamic frequency plan / filtering permits to adapt to drifts on the IF1 filter center frequency, while the OTA IIR filter can be reconfigured in terms of selectivity and gain. The simulation tool was key component on the frequency plan/filtering definition and optimization. The derived building blocks specifications are consistent with low power implementations described in the state of the art. This guarantees the compatibility of the proposed architecture with low power constraints. While defining the system level specifications on the proposed architecture, we figured out two critical points to be validated: the DT filtering implementation and the phase noise specifications which are at the core of the next two chapters of this thesis.

In order to lead an in-depth analysis of the DT filter implementation and to prove the feasibility, the IIR complex filter implementation is analyzed. The presented design flow consists in theoretical analysis of DT filtering processing, analytical development on the filter transfer function and behavioral modeling to apply parametrical simulations. The hypothesis that the DT receivers are robust to technology variation is observed while parameters such as capacitance mismatches and OTA finite gain and mismatch are evaluated on the filter. While we focus on the 65nm CMOS technology, the parametrical simulation is technology independent and is a robust technique for further technology migration of the circuit. The filter respects the specifications until σ_C=3% of capacitance mismatches and on 30% on the OTA open-loop gain A0. The choice of a unit capacitance of 50fF on the FIR stage lead to a σ_C=0.2% considering the ST 65nm technology. A feedback coefficient of β=0.8 is chosen, since it presents sufficient selectivity while no major impact is caused on the signal EVM. Limiting the open-loop gain, considering gm_{OTA}=5mS and the parasitic capacitances, the closed-loop gain is degraded by 4dB. On the I/Q mismatches, 5% gain and 5º phase shift are tolerated considering the specifications. The rotating OTA presents a strong feature to reduce gain mismatch on active blocks. Analytical noise figure analysis presents 2dB error compared to transient noise circuit level simulation, and the filter noise figure is 15dB over the sampler alone, therefore a gain stage is needed to compensate the impact on the SNR degradation.

Finally, the hypothesis of reducing the frequency synthesis power consumption while applying the BPS process is analyzed in detail in the last section of the thesis. More precisely, we

analyze if BPS represents or not an increasing on the jitter specifications constraints. We figured out that classical analysis considering uncorrelated jitter distribution and Nyquist sampling are not sufficient to understand the impact of jitter on the BPS process since different the synthesis jitter is more correlated than the opposite ($1/f^2$ noise or spur), and the under-sampling ratio aliases the impact of the jitter distortion into the Nyquist band. Analytical approach has been defined considering the BPS and a numerical method is proposed and validated in order to analyze different jitter distributions and signals. In order to set the phase noise specifications, empirical expressions considering a given test bench and the jitter type were developed. While evaluating the local SDjR, some non-intuitive conclusions appear, such as that the SDjR is independent on the under-sampling ratio in the case of correlated $1/f^2$ phase noise. In order to address the ULP RF channels, a non-fractional PLL needs a reference frequency of 1MHz; therefore, the phase noise spurious becomes a critical point to analyze. Finally, a PLL synthesis type is preferred rather than the DLL in order to reduce the impact of these spurs. The specifications on the BPS context referred to fs=98MHz are: $L_{fs}(\Delta f)$=-131.1dBc @ 3MHz and Δ_{SPURS}=-50.1dBc. These results show no particular power or implementation constraint on the PLL. Indeed, in this range of frequencies, the performance of PLL type synthesizer are greatly superior and present similar figure of merits than those around the RF frequency. Considering the average FoM and the defined specifications, the estimated power consumption on the VCO level is P_{VCO}=260µW, showing the great interest of relaxed system level constrains on the low power application. Considering classical architectures, the VCO power consumption is not really reduced, but the clock tree and the PLL buffers, while operating in an order of five times lower frequency, represent an important power economy. We remember that PPL in addition to the clock tree represent up to 40% of the receiver total power consumption.

Thanks to a DT-oriented design and the dynamic frequency plan, the proposed architecture enables agility in terms of technology migration and compensation of technology drifts, notably in the IF1 CT filter implementation. The IIR filter implementation permits to reconfigure the gain and selectivity with regards to an operation mode. Finally, harmful aliasing is avoided while decreasing the sampling frequency of the ADC, where the channel selection is completed. The derived specifications and results comparison with the state of the art show the low power characteristic of the proposed architecture. This is true notably due to the reduction on the clock tree and PLL frequencies, the relaxed constraints for the classical blocks, and the optimized frequency plan that permits to reduce the filtering techniques complexity.

2 List of Contributions

2.1 Conference Publications

[1] L. Lolis, et al., "System design of bandpass sampling RF receivers," in Electronics, Circuits, and Systems, 2009. ICECS 2009. 16th IEEE International Conference on, 2009, pp. 691-694.

[2] L. Lolis, et al., "Bandpass Sampling Rx System Design Issues and Architecture Comparison for Low Power RF Standards," in Circuits and Systems, 2010. ISCAS 2010. IEEE International Symposium on, 2010.

[3] L. Lolis, et al., "Impact of PLL 1/f2 and White Phase Noise in RF Bandpass Sampling Processing," in Circuits and Systems, 2010. NEWCAS 2010. IEEE Northeast Workshop on, 2010.

[4] L. Lolis, et al., "Ultra Low Power Bandpass Sampling Architectures Using Lamb Wave Filters," in Circuits and Systems, 2010. NEWCAS 2010. IEEE Northeast Workshop on, 2010.

[5] L. Lolis, et al., "A Bandpass Sampling Architecture Analysis for ULP Standards based on a Novel System Design Methodology," in Future Network and Mobile Summit Conference, 2010.

2.2 Patent

- L. Lolis and M. Pélissier, "Dispositif et procédé de réception de signaux RF basée sur une architecture hétérodyne à sous-échantillonnage IF complexe " France Patent 09 59216, 18 Dec, 2009.

2.3 Projects Deliverables

SENSEI Project

2.4 Journal Paper

- Agile RF Bandpass Sampling Receiver for Multistandard and Low Power Applications (to submit to TCAS)

2.5 Presentations, Seminars and non-reviewed reports

IEEE Seminar – Université des Trois Rivières Québec.

Workshop CEA – CSEM 2008 and 2009

3 Perspectives

The work presented in this thesis represents the definition of a new BPS architecture addressing both low power consumption and multistandard agility characteristics. Different methods and tools were developed for that matter and some improvements are possible. In order to improve the use of the state of the art as system level design chart, power consumption estimation models can be derived considering the figures of merit associated to a given base block and the data from the derived tables. This approach leads to an estimation of the power consumption directly from the retrieved performances for the blocks.

On the system design method, the constraints distributions were applied manually and updated considering design limitations. An optimization algorithm, possibly the geometric optimization, is interesting to be applied considering different distributions, calculating the required performances and evaluating the power consumption from the derived power estimation models. Current studies on the application of the geometric optimization on the system level design are being developed on classical architecture and has become of great interest of the system level designer's community. Possible improvements on the system simulation tool are observed as well. The system validation is based on local SNDR but can be extended to studies such EVM and BER if the modulation/demodulation blocks models are included. For that, increasing on the simulation speed is needed, by applying dynamic time step on the simulation environment and reducing the number of noise implementations per signal implementation. The inclusion on the tool of the developed numerical method of the last chapter will permit to evaluate phase noise impact on the BPS directly on the simulation tool.

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Glossary

ADC	*Analog to Digital Converter*
AMS	*Analog and Mixed Signal*
APP	*Application Processor*
ASIC	*Application-Specific Integrated Circuits*
B-LE	*Bluetooth Low Energy*
BER	*Bit Error Rate*
BPS	*Bandpass Sampling*
BAW	*Bulk Acoustic Wave*
BW	*Bandwidth*
C/H	*Charge-and-Hold*
CMOS	*Complementary Metal-Oxide-Semiconductor*
CT	*Continuous Time*
DBB	*Digital Base Band Processor*
DFT	*Discrete Fourier Transform*
DLL	*Delay-Locked Loop*
DSP	*Digital Signal Processor*
DSSS	*Direct Sequence Spread Spectrum*
DT	*Discrete Time*
DTTV	*Digital Terrestrial Television*
Eb/N0	*Energy per Bit to Noise Density*
EVM	*Error Vector Magnitude*
FD	*Frequency Divider*
FFT	*Fast Fourier Transform*
FIR	*Finite Impulse Response*
FPGA	*Field Programmable Gate Array*
FT	*Fourier Transform*
G·BW	*Gain Bandwidth Product*
Gv	*Voltage Gain*
I/Q	*In- and Quadrature- phase signals*
IF	*Intermediate Frequency*
IIP3	*Input Referred Third Order Intercept Point*
IIR	*Infinite Impulse Response*
IM3	*Third Order Intermodulation Product*
ISM	*Industrial, Scientific, and Medical*
LNA	*Low Noise Amplifier*
LWR	*Lamb Wave Resonators*
MAc	*Multiply-Accumulate*
MAC	*Media Access Control*
MMD	*Multi Modulus frequency Divider*
Nb_{eff}	*Effective Number of Bits*

NF	*Noise Figure*
OTA	*Operational Transconductance Amplifier*
PFD	*Phase Frequency Detector*
PLL	*Phase-Locked Loop*
PSD	*Power Spectral Density*
RF	*Radio Frequency*
RMS	*Root Mean Square*
S/H	*Sample-and-Hold*
SAR	*Successive Approximation Register*
SAW	*Surface Acoustic Wave*
SDR	*Software Defined Radio*
SDjR	*Signal-to-Jitter Distortion Ratio*
SDmR	*Signal-to-Mixing Distortion Ratio*
SNR	*Signal-to-Noise Ratio*
SNDR	*Signal-to-Noise-plus-Distortion Ratio*
SOA	*State of the Art*
TF	*TF*
ULP	*Ultra Low Power*
UWB	*Ultra Wide Band*
VCO	*Voltage Controlled Oscillator*
VGA	*Variable Gain Amplifier*
VHDL	*VHSIC Hardware Description Language*
VHSIC	*Very High Speed Integrated Circuits*
WBAN	*Wireless Personal Area Network*
WPAN	*Wireless Body Area Network*
WS&AN	*Wireless Sensor & Actuator Network*

Résumé Etendu

1 Introduction

La croissance des communications sans fils font émerger des besoins en terme d'architectures radiofréquences reconfigurables capables d'adresser de multiples standards tout en gardant une faible consommation électrique. Les nouvelles applications liées aux réseaux corporels sans fil (WBAN), réseaux personnels sans fil (WPAN), et réseaux de capteurs et actuateurs sans fil (WS&AN) s'appuyant sur des normes comme le Bluetooth Low Energy et IEEE802.15.4 par exemple sont exigeantes sur le plan de la consommation électrique. Ces standards constituent le point de départ de notre analyse. Dans ce contexte, l'objectif de la thèse est de proposer et dimensionner une nouvelle architecture capable d'adresser les problématiques de multistandard et de basse consommation. Le choix s'est portée sur une architecture basée sur la technique de sous échantillonnage, qui permet d'exploiter un certain nombre d'avantages associés au traitement du signal en temps discret. Dans un contexte multistandard, la radio logicielle offre un maximum de flexibilité. En effet, l'échantillonnage et le traitement numérique du signal peuvent s'effectuer le plus près possible de l'antenne. Malheureusement, les performances requises par le convertisseur analogique numérique ne sont pas adaptées à la basse consommation électrique. Afin de réduire la consommation, les techniques à base de sous échantillonnage du signal radio semblent offrir d'excellentes perspectives. Le principe s'appuie sur l'échantillonnage de la bande utile et de l'information associée plutôt que du signal porteur. La cadence des circuits de synthèse de fréquence et d'échantillonnage est par conséquent réduite. Finalement, les performances du convertisseur analogique numérique peuvent être relâchées grâce à des opérations de filtrage en temps discret et de décimation. Ces techniques de filtrage sont adaptées au changement de la fréquence d'échantillonnage ce qui permet d'offrir de la flexibilité au niveau de l'architecture. Néanmoins, il existe des limitations en terme de repliement du spectre et de produit gain bande du circuit d'échantillonnage. Ces limitations peuvent être maitrisées dans un contexte applicatif ou les contraintes en termes de réjection d'interféreurs sont plus relâchées que dans un réseau de type cellulaire par exemple.

2 La méthode de conception système et l'outil de simulation système

Afin d'appréhender ces nouvelles contraintes, il est apparu nécessaire de développer un outil de simulation système sous Matlab modélisant la chaîne de réception sur une large bande spectrale (Figure 3-14). Le principal intérêt de cet outil est de mettre en évidence le repliement des interféreurs dans la bande Radio Fréquences du standard, afin de définir le plan fréquentiel, répartir les contraintes en filtrage, ainsi que les performances des blocs du récepteur. L'outil permet de discriminer les différentes sources de distorsion du signal (bruit, non linéarité, repliement d'interféreurs, bruit de phase). Grâce à cela, il est possible de redistribuer les contraintes associées aux différents blocs (NF,G,IP3) pour relâcher les spécifications critiques en termes de consommation. Ensuite, une méthode de spécification système adaptée au processus de sous échantillonnage a été mise en place afin de converger rapidement vers une configuration optimisée des performances par blocs (Figure 3-10). La redistribution des contraintes prend en compte à la fois les besoins des normes de communication (approche top-down) et les limitations circuit (approche bottom-up).

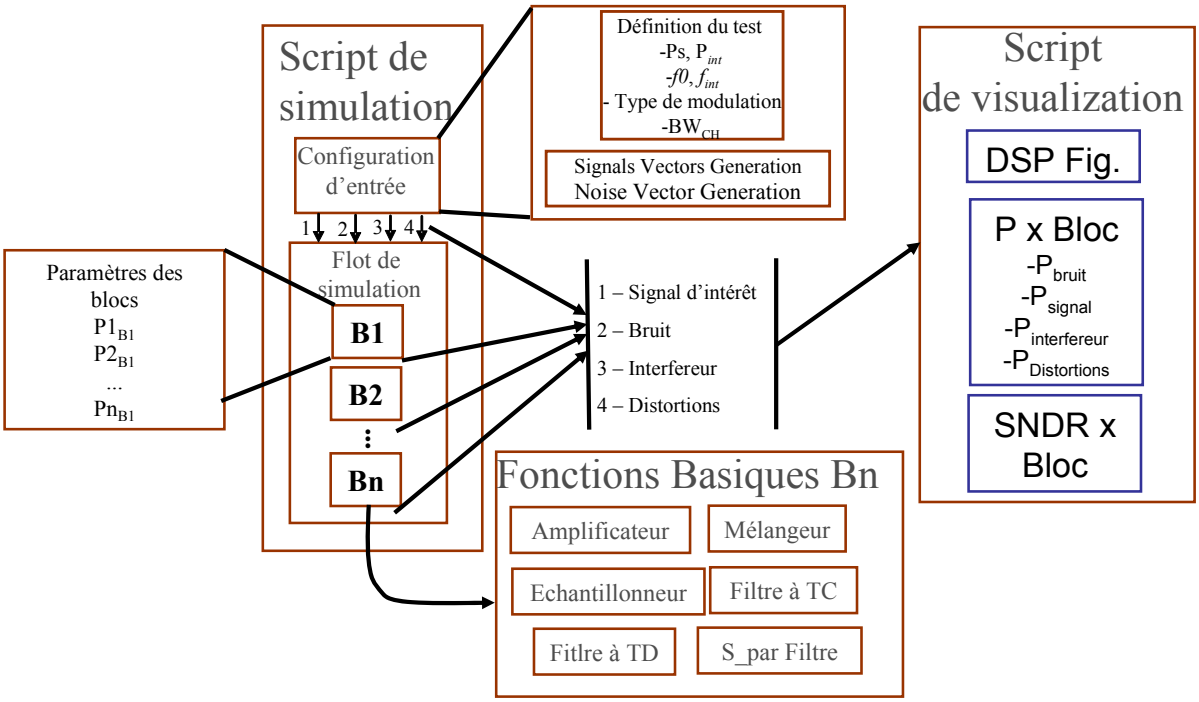

Figure 1 : Digramme de bloc de l'outil de simulation système

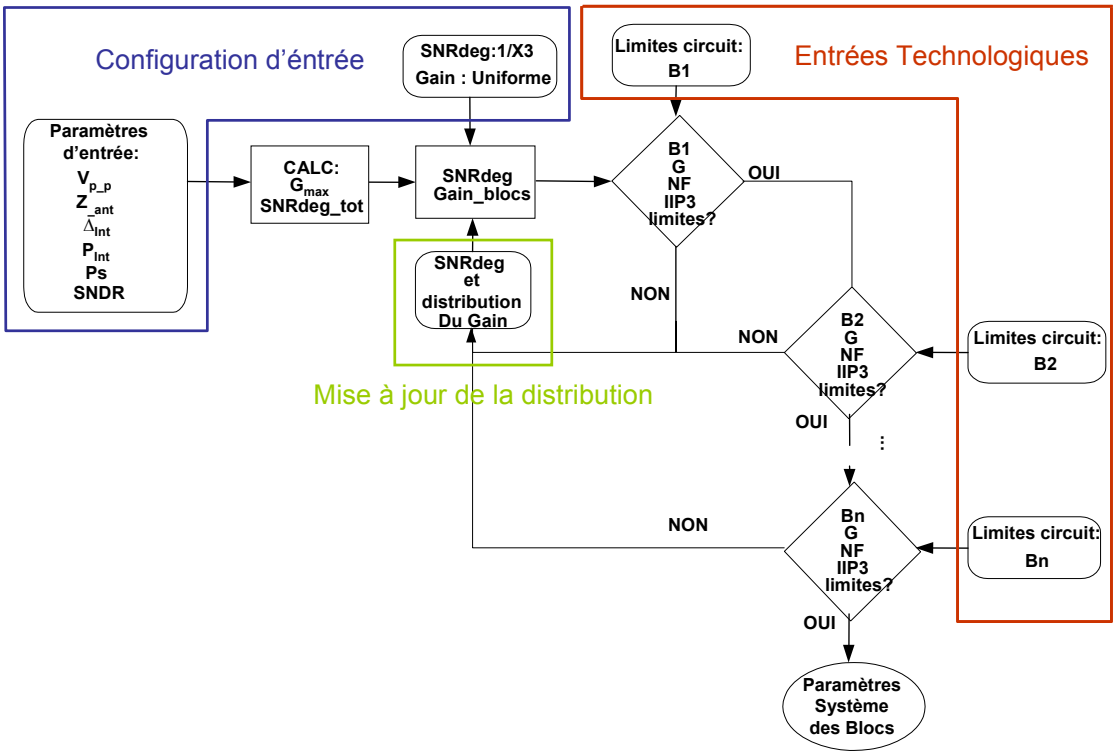

Figure 2 : La méthode de simulation système propose

3 Comparaison quantitative et définition d'une nouvelle architecture de réception à sous échantillonnage

A l'aide de l'outil et de la méthode associée mis au point, une comparaison quantitative a été menée pour différentes architectures à sous échantillonnage. Une attention particulière a été portée sur l'optimisation du filtrage dans la chaîne entre les éléments à temps continu (BAW, Ondes de Lamb) et à temps discret (capacités commutées à réseaux actifs ou passifs). Le choix des fréquences intermédiaires s'est avéré primordial dans cette optimisation. Les normes visées Bluetooth Low Energy et IEEE802.15.4, présentent des contraintes en rejection modérées et autorisent l'utilisation de techniques de filtrage à temps continu, à temps discret, ou d'un mixte des deux. L'étude a conduit à proposer une nouvelle architecture (Figure 4-25) de réception sous échantillonnée par laquelle l'application d'un filtrage à temps continu à haute fréquence intermédiaire et d'un filtrage complexe à temps discret vers une basse fréquence intermédiaire, représente le meilleur compromis consommation - agilité. Deux avantages majeurs ressortent de cette architecture: de basses fréquences de référence pour la conversion en fréquence, et une implémentation simplifiée des techniques de filtrage en temps continu et discret.

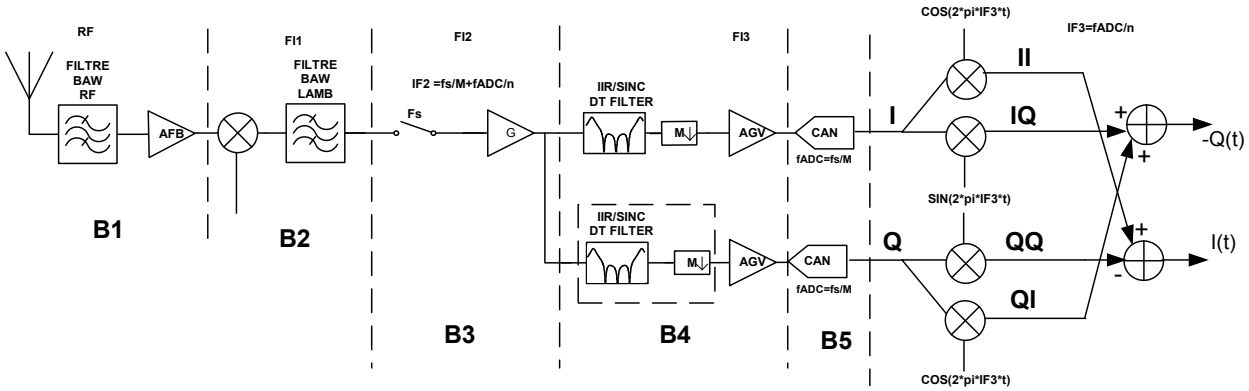

Figure 3 : Architecture à haute FI1, filtre à temps continu à FI1 et sous échantillonnage en tension, filtre complexe à temps discret à FI2

4 Implémentation du filtre complexe à temps discret à RII

La fonction de filtrage complexe à temps discret à réponse impulsionnelle infinie (RII) est un élément clé de l'architecture. Dans cette partie de la thèse, l'objectif est d'évaluer l'impact des imperfections du circuit et de valider la fonction de transfert du filtre à réseau de capacités. Une modélisation du réseau de filtrage a été développée en langage VHDL-AMS (Figure 4 et Figure 5) afin de prendre en compte les contraintes d'implémentation au plus proche du circuit tel que les capacités parasites, bruit et distorsion de Switch. L'objectif est de garantir un fonctionnement global de l'architecture, spécifier les tolérances possibles sur les capacités et transistor de Switch du réseau. Un développement analytique de la fonction de transfert en bruit a été mené pour dimensionner les capacités du réseau de filtrage. Enfin, on a étudié l'application d'amplificateurs opérationnels à transconductance comme étage de sortie du filtre. Le modèle comportemental a permis de spécifier la transconductance et l'impédance de sortie d'un tel bloc tout en minimisant sa consommation.

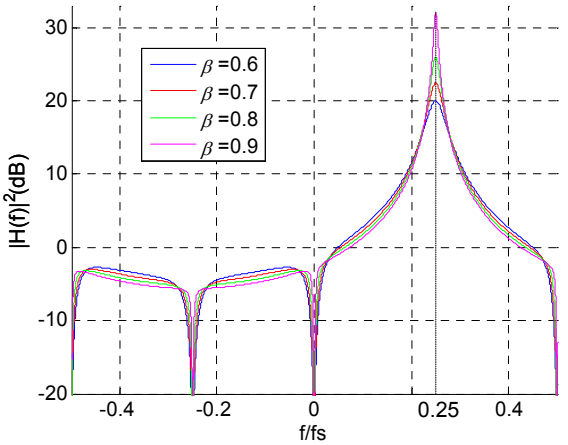

Figure 4 : Gain vs f/fs for the complex IIR filter

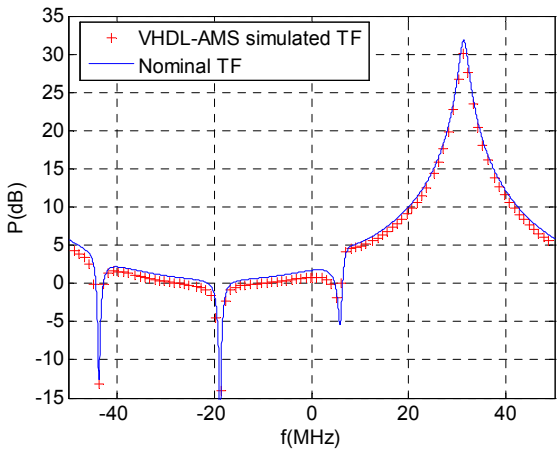

Figure 5 : Sampled signal normalized PSD and the filter theoretical TF

5 Spécifications en bruit de phase pour l'architecture proposée

Par la suite, une analyse détaillée sur la synthèse de fréquence a été conduite. En effet, les circuits de synthèse de fréquence peuvent représenter jusqu'à 30% du budget de consommation d'un récepteur Radio Fréquences. Il est important de savoir si le processus de sous échantillonnage représente une contrainte supplémentaire en terme de bruit de phase et quel bénéfice peut on attendre au niveau synthèse de fréquence de telle technique. Une étude approfondie de l'impact du jitter d'horloge sur la distorsion du signal sous échantillonné a été menée. Pour répondre à ce besoin, une nouvelle méthode numérique a été proposée, capable d'évaluer le rapport signal sur distorsion due au jitter (*SDjR*), dans le processus de sous échantillonnage. La méthode est basée sur l'interpolation du signal discret pour évaluer ça valeur dans des instants non définis par la simulation, et que représentent l'échantillonnage en présence du jitter (Figure 6-5). On a constaté que le *SDjR* est proportionnel à la variance du jitter et ne dépend pas directement de la pureté spectrale. Cela signifie que sous échantillonner n'impose pas de contrainte particulière en bruit de phase (Figure 6-11). Par contre la fréquence à générer étant plus faible, il en résulte une réduction de la consommation des étages de sortie du circuit de synthèse de fréquence. Finalement les spécifications en bruit de phase sont dégagées concernant l'architecture proposée référencées à une synthèse à 98MHz (Tableau 14).

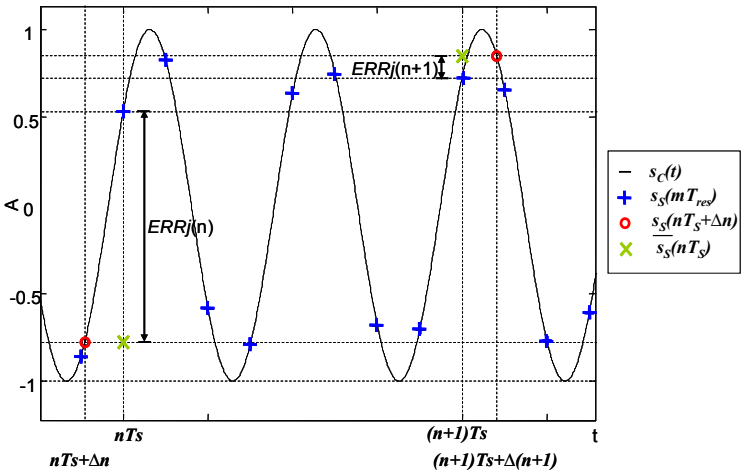

Figure 6 : L'interpolation et la représentation du signal continu, $s_c(t)$, simulé $s_s(mT_{res})$, et interpolé pour les instants d'échantillonnage en présence de jitter ($\overline{s_s(nTs)}$)

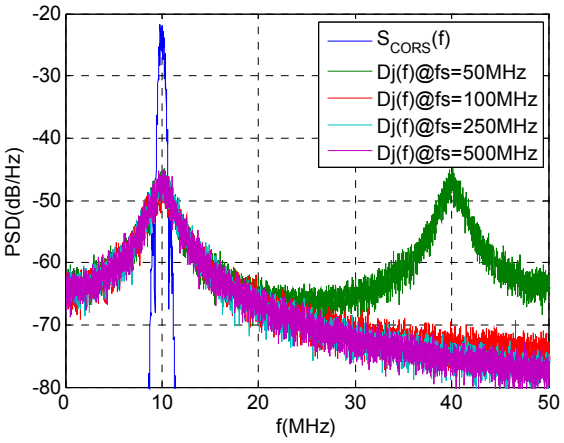

Figure 7 : $S_{CORS}(f)$ and Dj(f)

Paramètres	**L_{fs}(3MHz)**	**Δ_{spur_fs}(3MHz)**	**σ_{AP}**	**fn**
Valeur	-133.3dBc	-74dBc	24ps	175KHz

Tableau 14- Spécifications en bruit de phase

6 Conclusions générales

Vis-à-vis des résultats ici présentés on a montré l'importance de maîtriser les nouvelles contraintes système lors du processus de sous échantillonnage. On constate qu'il est possible de proposer des architectures de réception radiofréquence à sous échantillonnage à complexité réduite capable de répondre aux aspects multistandard basse consommation. La modélisation comportementale a permis de valider les performances et la faisabilité des réseaux de filtrage à temps discret. Finalement, le plan fréquentiel proposé a permis de réduire la consommation des blocs de synthèse de fréquence. Le circuit proposé issu des spécifications est en cours de design dans l'équipe projet au sein du LETI.

Agile Bandpass Sampling RF Receivers for low power Applications

Abstract: New wireless communications pushes the development in terms reconfigurable, multistandards and low power radio systems. This work proposes and design new receiver architecture capable of addressing these aspects. The Bandpass Sampling (BPS) is applied and permits to exploit a certain number of advantages linked to the discrete time (DT) signal processing, notably filtering and decimation, relaxing the ADC constraints and keeping the multi standard and reconfigurable features. A developed wide band system level simulation tool and system design method permit to overcome system level limitations such spectral aliasing, separating the different contributions on the SNDR degradation, splitting the blocks constraints and defining the optimum frequency plan and filtering. The proposed BPS architecture on the thesis is a result of a quantitative comparison of different BPS architectures, applying the system design method and tool, and represents the best trade-off between power consumption and agility on the aimed context. The DT filtering block is identified as critical block. Effects such parasitic capacitances and capacitance mismatch, switch noise, finite gain OTA, are evaluated through VHDL-AMS modelling. It is observed the robustness of discrete time oriented circuits. Finally, phase noise specifications are given considering that frequency synthesis circuits may represent up to 30% of the power consumption. For that goal, a new numerical method is proposed to evaluate the signal to jitter distortion ratio *SDjR* on the BPS process. Moreover, a non intuitive conclusion is given, where reducing the sampling frequency does not increase the constraints in terms of jitter. The proposed architecture is in stage of circuit level design for proof of concept.

Résumé: Les nouveaux besoins en communications sans fil pussent le développement de systèmes de transmission RF en termes the reconfigurabilité, multistandard et à basse consommation. Cette thèse propose d'une nouvelle architecture de réception capable d'adresser ces aspects. Le sous échantillonnage est appliquée et permet d'exploiter et certain nombre d'avantages liées au traitement du signal à Temps Discret, notamment le filtrage et la décimation, permettant de relâcher les contraintes liées aux ADCs en maintenant des caractéristiques multistandard et de reconfigurabilité. Un simulateur large bande développé et une nouvelle méthode ce conception système permettent répondre à des limitations au niveau système comme le repliement spectral, séparer les différentes contributions dans la dégradation du SNDR, séparer les différentes contraintes des blocs pour la définition d'un plan de fréquence et the filtrage optimaux. L'architecture à sous échantillonnage proposée dans la thèse est résultat d'une comparaison quantitative des différentes architectures à sous échantillonnage, tout en appliquant la méthode et l'outil de conception système développés; et représente le meilleur compromis entre la consommation électrique et l'agilité, dans le contexte voulu. Le bloc de filtrage à temps discret est identifié comme étant critique. Des effets come les capacités parasites, l'imparité entre les capacités, le bruit du commutateur, le gain finit de Ampli OP, sont évalués à travers d'une simulation comportementale en VHDL-AMS. On observe la robustesse des circuits orientés temps discret par rapport les contraintes des nouvelles technologies intégrés. Finalement, le système est spécifié en termes de bruit de phase, qui peuvent représenter jusqu'à 30% de la consommation en puissance. Dans ce but, une nouvelle méthode numérique est proposée pour évaluer le rapport signal sur distorsion due au jitter *SDjR* dans le processus de sous échantillonnage. En plus, une conclusion non intuitive est survenue de cette étude, où on que réduire la fréquence d'échantillonnage n'augmente pas les contraintes en termes de jitter pour le système. L'architecture proposée issue de cette étude est sujet d'un développement circuit pour la validation du concept.